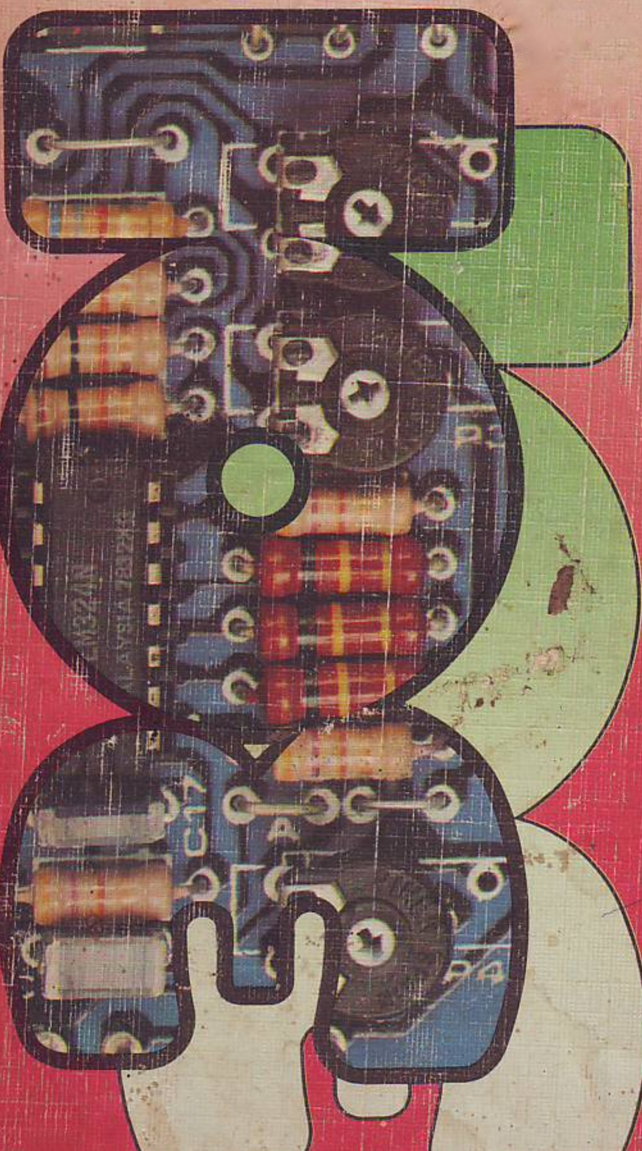
301 circuits

Circuits 1 to 78



Vol - 1

AN
elektor
PUBLICATION

301 circuits

practical
electronic circuits
for the home
constructor

introduction

301 circuits

The book follows the theme, and is a continuation of our popular and very successful 300 circuits publication. It is composed of 301 assorted circuits ranging from the simple to the more complex designs described and explained in straightforward language. An ideal basis for constructional projects and a comprehensive source of ideas for anyone interested in electronics. In a nutshell something to please everybody.

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Semiconductor types
Very often, a large number of equivalent semiconductors exist with different type numbers. For this reason, 'abbreviated' type numbers are used in Elektor wherever possible:

- '741' stand for μA 741, LM 741, MC 741, MIC 741, RM 741, SN 72741, etc.
- 'TUP' or 'TUN' (Transistor, Universal, PNP or NPN respectively) stand for any low frequency silicon transistor that meets the following specifications:

$U_{CEO,max}$	20 V
$I_{C,max}$	100 mA
$h_{fe,min}$	100
$P_{tot,max}$	100 mW
$f_{T,min}$	100 MHz

Some **'TUN'**s are: BC 107, BC 108 and BC 109 families; 2N3856A, 2N3859, 2N3860, 2N3904, 2N3947, 2N4124.
Some **'TUP'**s are: BC 177 and BC178 families; BC179 family with the possible exception of BC 159 and BC 179; 2N2412, 2N3251, 2N3906, 2N4126, 2N4291.

- 'DUS' or 'DUG' (Diode Universal, Silicon or Germanium respectively) stands for any diode that meets the following specifications:

	DUS	DUG
$U_{R,max}$	25 V	20 V
$I_{F,max}$	100 mA	35 mA
$I_{R,max}$	1 μA	100 μA
$P_{tot,max}$	250 mW	250 mW
$C_{D,max}$	5 pF	10 pF

Some **'DUS's** are: BA 127, BA 217, BA 218, BA 221, BA 222, BA 317, BA 318, BAX 13, BAY 61, 1N914, 1N4148.

Some **'DUG's** are: OA 85, OA 91, OA 95, AA 116.

- 'BC 107B', 'BC 237B', 'BC 547B' all refer to the same 'family' of almost identical better-quality silicon transistors. In general, any other member of the same family can be used instead.

BC 107 (-8, -9) families
BC 107 (-8, -9), BC 147 (-8, -9), BC 207 (-8, -9), BC 237 (-8, -9), BC 317 (-8, -9), BC 347 (-8, -9), BC 547 (-8, -9), BC 171 (-2, -3), BC 182 (-3, -4), BC 382 (-3, -4), BC 437 (-8, -9), BC 414

BC 177 (-8, -9) families
BC 177 (-8, -9), BC 157 (-8, -9), BC 204 (-5, -6), BC 307 (-8, -9), BC 320 (-1, -2), BC 350 (-1, -2), BC 557 (-8, -9), BC 251 (-2, -3), BC 212 (-3, -4), BC 512 (-3, -4), BC 261 (-2, -3), BC 416.

Resistor and capacitor values
When giving component values, decimal points and large numbers of zeros are avoided wherever possible. The decimal point is usually replaced by one of the following abbreviations:

p	(pico-)	$= 10^{-12}$
n	(nano-)	$= 10^{-9}$
μ	(micro-)	$= 10^{-6}$
m	(milli-)	$= 10^{-3}$
k	(kilo-)	$= 10^{3}$
M	(mega-)	$= 10^{6}$
G	(giga-)	$= 10^{9}$

A few examples:
Resistance value 2k7: 2700 Ω.
Resistance value 470: 470 Ω,
Capacitance value 4p7: 4.7 pF, or 0.000 000 000 004 7 F . . .
Capacitance value 10 n: this is the international way of writin writing 10,000 pF or .01 μF, since 1 n is 10^{-9} farads or 1000 pF.

Resistors are ¼ Watt 5% carbon types, unless otherwise specified. The DC working voltage of capacitors (other than electrolytics) is normally assumed to be at least 60 V. As a rule of thumb, a safe value is usually approximately twice the DC supply voltage.

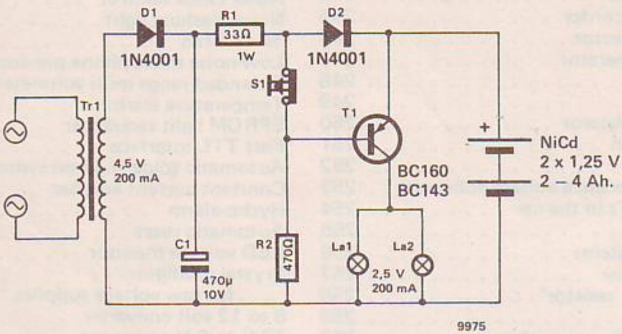
Test voltages
The DC test voltages shown are measured with a 20 kΩ/V instrument, unless otherwise specified.

U, not V
The international letter symbol 'U' for voltage is often used instead of the ambiguous 'V'. 'V' is normally reserved for 'volts'. For instance: $U_b = 10$ V, not $V_b = 10$ V.

Mains voltages
No mains (power line) voltages are listed in Elektor circuits. It is assumed that our readers know what voltage is standard in their part of the world!
Readers in countries that use 60 Hz should note that Elektor circuits are designed for 50 Hz operation. This will not normally be a problem; however, in cases where the mains frequency is used for synchronisation some modification may be required.

contents

1 Automatic emergency lighting unit



This unit charges a nickel-cadmium battery from the mains to provide a standby power supply for emergency lighting in the event of a mains failure. When the mains supply drops out, the lighting is switched on automatically.

The circuit of the unit is extremely simple. Tr1, D1 and C1 provide a halfwave rectified and smoothed DC supply of approx. 6 V, which is used to continuously charge the Ni-Cad battery at about 100 mA via R1 and D2. A 2 Ah Ni-Cad can safely be charged at this rate.

The voltage drop across D2 reverse-biases the base-emitter junction of T1, so that this transistor is turned off and the lamps are not lit. When the mains supply fails, however, T1 is supplied with base current via R2; the transistor therefore turns on and the lamps are lit. As soon as the mains supply is restored, T1 will turn off, the lamps are extinguished and the battery is once more charged via R1 and D2.

The unit can be mounted wherever emergency lighting will be required in the event of a power failure. An obvious example is in that infamous dark cupboard under the stairs, so that, should a fuse blow, a replacement can be easily found and fitted.

A transformer with a slightly higher secondary voltage can be used, provided that R1 is uprated to limit the current through this resistor to 100 mA.

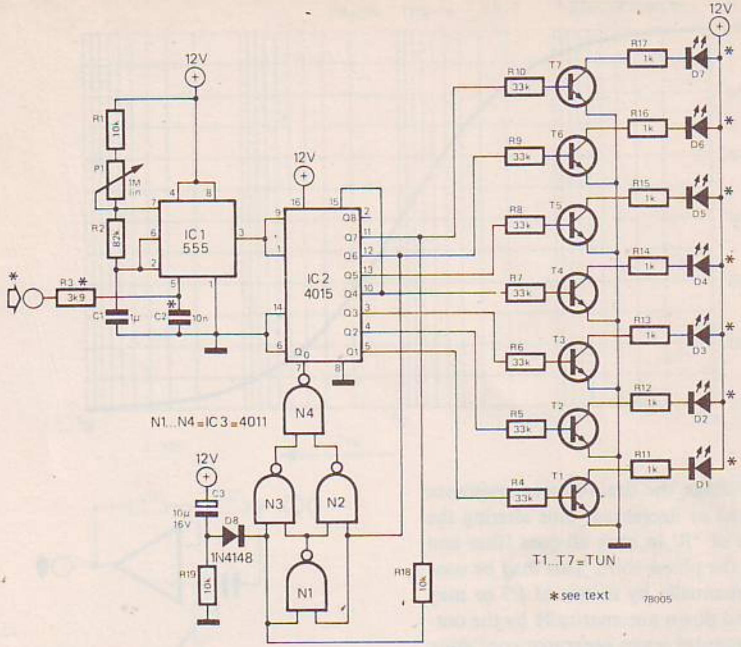
2 Pseudo random running lamp

If a number of the outputs of a shift register are fed back in a certain fashion via an EXOR gate to the data input, then the Q outputs of the register will run through the maximum possible number of mutually different logic states. By using the Q outputs to drive LEDs a visual representation of the truth table for a shift register with EXOR feedback is obtained. At each clock pulse a logic '1' (LED lights up) or '0' moves up one place, so that the net result is a running light.

In this circuit the Q outputs of the shift register (IC2), which is seven bits long, are routed via an EXOR gate (N1...N4) back to pin 7, the data input, of the register. The clock signal is provided by IC1. The clock frequency, and hence the speed of the running light, can be altered by means of P1. R4...R17 and T1...T7 are included to drive the LEDs. R18, R19, C3 and D8 ensure that when the circuit is switched on, a logic '1' appears at the data input, which means that the register output state can never be all zeroes.

The circuit can be extended for use as a light organ. The LEDs are replaced by opto-couplers which, via the necessary hardware (triac etc.) control incandescent lamps.

A rectified version of the audio signal is fed via R3 to the control input of IC1, where it is used to modulate the clock frequency of the register and



hence the speed of the running light. Capacitor C2 may then be omitted. Varying the control voltage between 0 and 15 V will result in the clock frequency being varied between 50 and 150% of the value obtained with the control input left floating.

3 Phaser

In contrast to lowpass or highpass filters, the gain of an all-pass filter remains constant over the range of frequencies at which it is used, but it does introduce a frequency-dependent phase shift. A number of all-pass filters may be cascaded to produce a phasing unit for use in electronic music. The phasing effect is produced by phase-shifting a signal and then summing the original and phase-shifted versions of the signal.

Figure 1 shows the basic circuit of a first order all-pass filter. The phase-shift is dependent on the relative values of R and C and on the input frequency. At low frequencies C has a very high impedance and the circuit simply functions as an inverting amplifier, so the phase-shift is 180°. At high frequencies the impedance of C is low and the circuit functions as a non-inverting amplifier with zero phase-shift.

The gain of the filter depends on the relative values of R1 and R2. In this case R1 and R2 are chosen equal so that the gain is unity. The graph shows the phase-shift v. frequency curve for the filter.

The complete circuit of a phasing unit using all-pass filters is shown in figure 2. Six all-pass filter stages are cascaded, so the total phase-shift at low frequencies can be up to 1080°! The use of a total of ten op-amps in the circuit may seem rather excessive, but as eight of these are LM324 quad op-amps the total package count is only four ICs.

IC1a functions as a unity gain input buffer and IC1b to IC2c are the six filter stages. The direct and phase-shifted signals are summed by IC2d. The proportion of phase-shifted signal and hence the depth of phasing can be adjusted by means of P4.

The degree of phase-shift at a particular frequency can be varied by FETs T1 to T6, which function as voltage controlled resistors. By vary-

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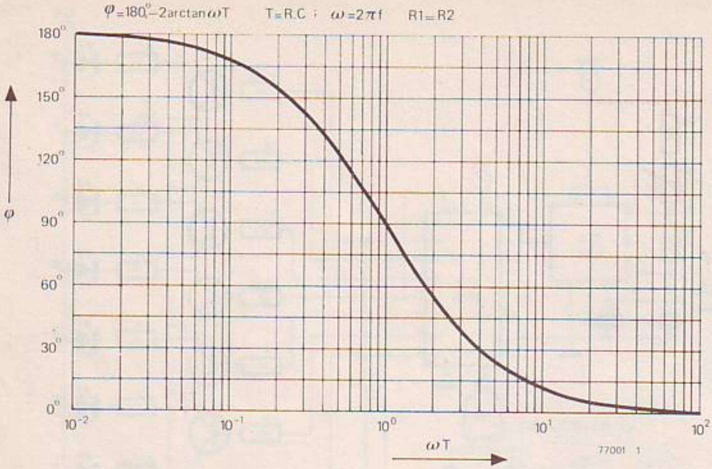
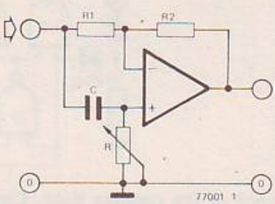


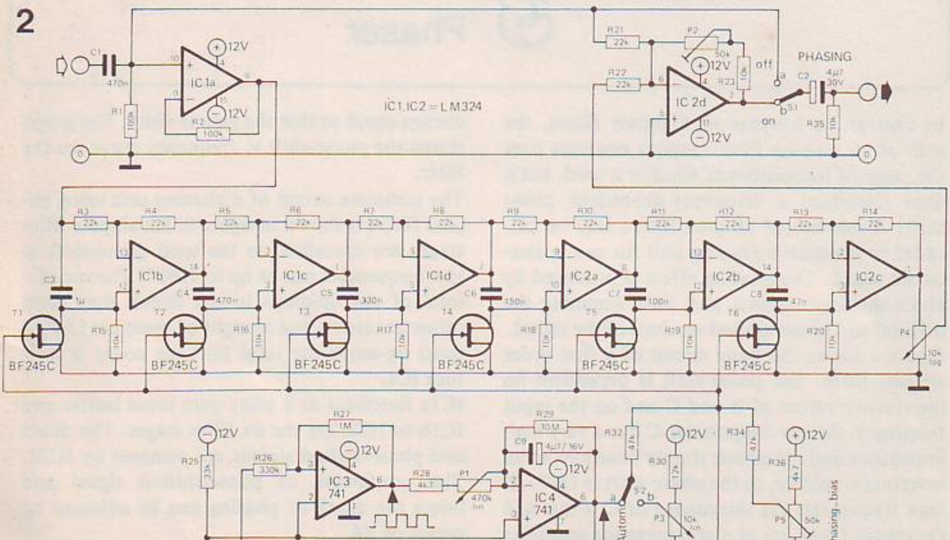
ing the gate voltage the drain-source resistance can be increased or decreased, thus altering the effective value of 'R' in each all-pass filter and hence varying the phase-shift. This may be controlled either manually by means of P3 or may be swept up and down automatically by the output of the triangular wave generator consisting of IC3 and IC4. As the gate voltage of the FETs must always be negative the output of this oscillator swings between − 2 and − 6 V.

The oscillator frequency may be varied by means of P1, and the best phasing effect occurs at fre-



quencies between 0.5 Hz and 1 Hz. At higher frequencies (around 4 Hz) the phasing effect is lost but a vibrato effect is obtained instead.

2



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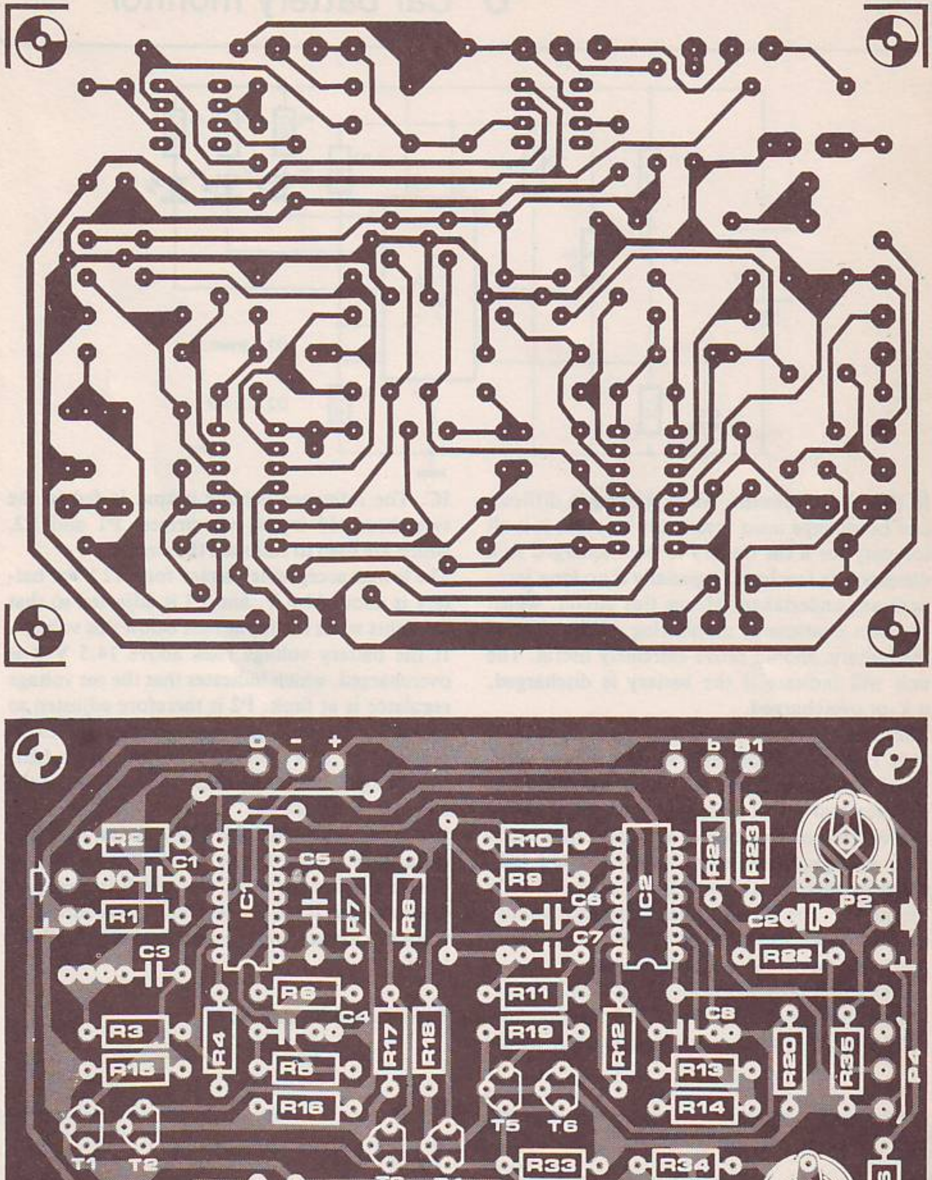
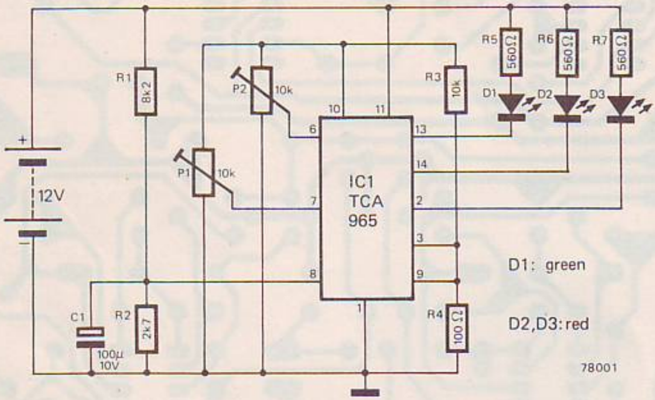


0 - +
a b S1
R2
C1
R1
C3
IC1
C5
R7
R8
R6
C4
R3
R15
R4
R5
R16
R17
R18
T1
T2
T3
T4
R10
R9
C6
C7
IC2
R21
R23
P2
C2
R22
R11
R19
R12
C8
R13
R14
R20
R35
P4
T5
T6
R33
R34
R36
P5
R25
R24
IC3
R27
R28
C9
R29
IC4
R32
R31
R30
R26
P1
a S2 b
P3

4 Car battery monitor



In the winter months, when starting is difficult and headlamps must frequently be used, it is all too easy for a car battery to be discharged to a dangerously low level, especially if no long journeys are undertaken. Hence this circuit, which provides continuous monitoring of the state of the battery, should prove extremely useful. The unit will indicate if the battery is discharged, o.k. or overcharged.

The circuit is based on the Siemens IC type TCA 965. This IC is a complete window comparator, which will indicate whether the input voltage lies between two preset reference voltages, is below the low reference voltage or above the high reference voltage. These three conditions are indicated by three LEDs, which are driven directly by the IC. The IC also has a reference voltage output, which can be used to derive the upper and lower thresholds of the 'window'.

The circuit is powered from the 12 V car battery, and the battery voltage is also fed, via potential divider R1/R2, to the monitoring input of the IC. The reference voltage output is fed to the two threshold inputs via presets P1 and P2, which are used to calibrate the circuit.

The lowest acceptable voltage for a 12 V car battery is about 11.5 V, and P1 is adjusted so that D1 lights when the input falls below this voltage. If the battery voltage rises above 14.5 V it is overcharged, which indicates that the car voltage regulator is at fault. P2 is therefore adjusted so that D3 is lit for input voltages above 14.5 V. Between 11.5 V and 14.5 V the green LED should light, indicating that the condition of the battery is satisfactory.

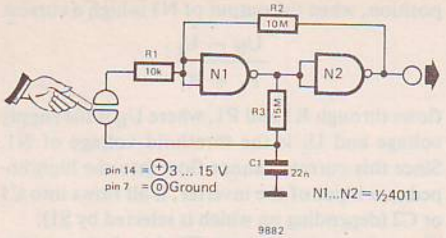
It will be noticed that the LEDs do not light and extinguish at exactly the same voltage. This is due to a hysteresis of 60 mV which is incorporated into the IC to prevent the LEDs flickering when the battery voltage is close to the threshold levels.

Siemens Application Note

5 TAP-tip

Many circuits for TAPs (Touch Activated Programme switches) have previously been published. However, all of these required the use of two pairs of touch contacts, one to set the TAP to the 'on' position and one to reset it to the 'off' position. The novel feature of this circuit is that it requires only one touch contact. Touching the contact once sets the TAP; touching it a second time resets the TAP.

N1 and N2 form a flip-flop (bistable multivibrator). Assume that initially the output of N2 is low. The inputs of N1 are also pulled low via R2,



so the output of N1 is high. The inputs of N2 are thus high, which satisfies the criterion for the output to be low, which was the original assumption. C1 is charged to logic high through R3 from the high output of N1. If the touch contacts are now bridged by a finger, the logic high on C1 will be applied to the inputs of N1 through R1 and the skin resistance. The output of N1 will go low, so the output of N2 will go high, holding the inputs of N1 high even if the finger is removed. The TAP is now set.

Once the finger is removed, C1 will discharge through R3 into the low output of N1. If the touch contacts are subsequently bridged, the inputs of N1 will be pulled low by C1 (since it is now discharged). The output of N1 will thus go high and the output of N2 low, which will hold the inputs of N1 low even after the finger has been removed. The TAP is now reset to its original state. C1 will charge to logic high through R3 from the output of N1, ready for the contact to be touched again.

The only constraint on the operation of the circuit is that the interval between successive operations of the switch must be at least half a second to allow C1 time to charge and discharge.

6 CMOS function generator

Using only one inexpensive CMOS IC and a handful of discrete components, it is possible to build a versatile function generator that will provide a choice of three waveforms over the entire audio spectrum and beyond.

The aim of this project was to produce a simple, cost-effective, general purpose audio generator, which was easy to build and use. This aim has certainly been achieved, since the circuit offers a choice of sine, square and triangle waveforms and a frequency range from about 12 Hz to 70 kHz, yet uses only one CMOS hex inverter IC and a few discrete components. Of course, the design does not offer the performance of more sophisticated circuits, particularly as regards waveform quality at higher frequencies, but it is nonetheless an extremely useful instrument for audio work.

Block diagram

Figure 1 illustrates the operating principles of the circuit. The heart of the generator is a triangle/squarewave generator consisting of an integrator and a Schmitt trigger. When the output of the Schmitt trigger is high, the voltage fed back from the Schmitt output to the input of the integrator causes the integrator output to ramp negative until it reaches the lower trigger threshold of the Schmitt trigger. At this point the output of the Schmitt trigger goes low, and the low voltage fed back to the integrator input causes it to ramp positive until the upper trigger threshold of the Schmitt trigger is reached. The output of the Schmitt trigger again goes high, and the integrator output ramps negative again, and so on. The positive- and negative-going sweeps of the integrator output make up a triangular waveform, whose amplitude is determined by the hysteresis of the Schmitt trigger (i.e. the difference between the upper and lower trigger thresholds). The output of the Schmitt trigger is, of

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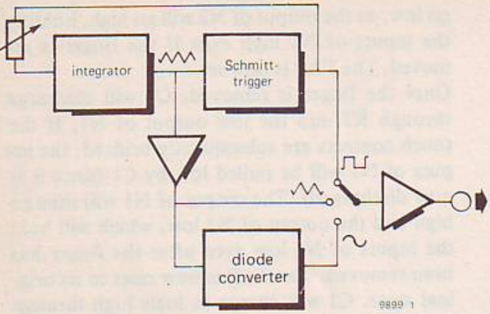

course a square wave consisting of alternate high and low output states.

The triangle output is fed through a buffer amplifier to a diode shaper, which 'rounds off' the peaks and troughs of the triangle to produce an approximation to a sinewave signal.

Any one of the three waveforms may then be selected by a three-position switch and fed to an output buffer amplifier. The frequency of all three signals is varied by altering the integrator time constant, which changes the rate at which the integrator ramps, and hence the signal frequency.

Complete circuit

The practical circuit of the CMOS function generator is given in figure 2. The integrator is based on a CMOS inverter, N1, whilst the Schmitt trigger uses two inverters with positive feedback, N2 and N3.

The circuit functions as follows; assuming, for the moment, that the wiper of P2 is at its lowest position, when the output of N3 is high a current

$$\frac{U_b - U_t}{P_1 + R_1}$$

flows through R1 and P1, where U_b is the supply voltage and U_t is the threshold voltage of N1. Since this current cannot flow into the high impedance input of the inverter, it all flows into C1 or C2 (depending on which is selected by S1).

The voltage drop across C1 thus increases linearly, so the output voltage of N1 falls linearly until the lower threshold voltage of the Schmitt trigger is reached, when the output of the Schmitt trigger goes low. A current

$$\frac{-U_t}{P_1 + R_1}$$

now flows through R1 and P1. This current also flows into C1, so the output voltage of N1 rises linearly until the upper threshold voltage of the Schmitt trigger is reached, when the output of the Schmitt trigger goes high and the whole cycle repeats.

To ensure symmetry of the triangle waveform (i.e. the same slope on both positive-going and negative-going portions of the waveform) the charge and discharge currents of the capacitor must be equal, which means that $U_b - U_t$ must equal U_t. Unfortunately U_t is determined by the characteristics of the CMOS inverter and is typically 55% of supply voltage, so $U_b - U_t$ is about 2.7 V with a 6 V supply and U_t is about 3.3 V.

This difficulty is overcome by means of P2, which allows symmetry adjustment. Assume for the moment that R – is connected to the positive

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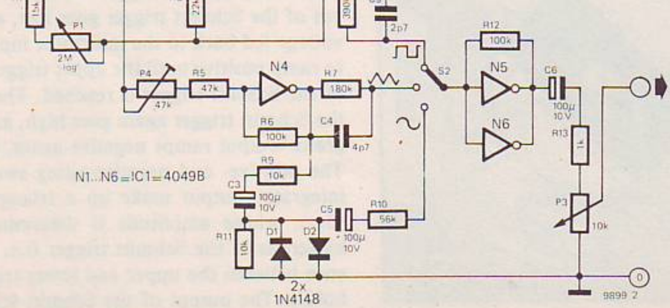
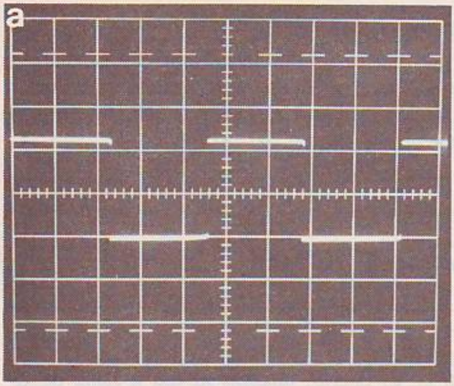
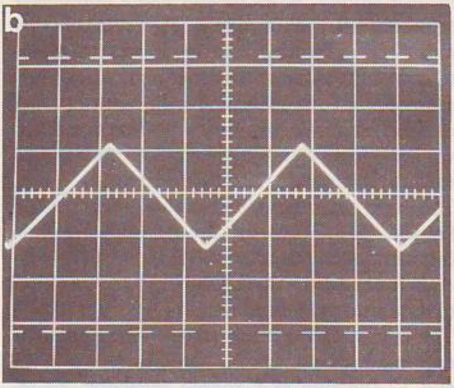


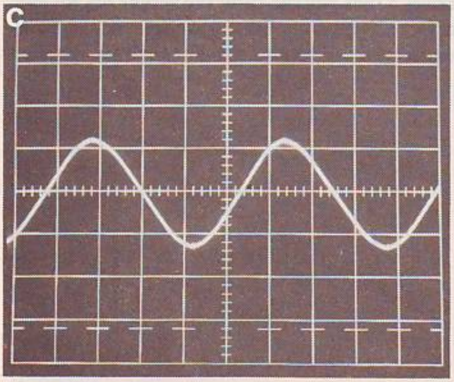
Figure 1. Block diagram of the CMOS function generator.

Figure 2. Complete circuit of the function generator.

Photos. The three output waveforms produced by the function generator.







supply rail (position A). Whatever the setting of P2, the high output voltage of the Schmitt trigger is always U_b. However, when the output of N3 is low, R4 and P2 form a potential divider so that a voltage from 0 V to 3 V can be fed back to P1, depending on the wiper setting of P2. This means that the voltage across R1 and P1 is no longer $-U_t$ but $U_{P_2} - U_t$. If the slider voltage of P2 is about 0.6 V then $U_{P_2} - U_t$ will be around -2.7 V, so the charge and discharge currents will be the same. Of course, the adjustment of P2 must be carried out to suit each individual function generator, owing to the tolerance in the value of U_t. In cases where U_t is less than 50% of the supply voltage, it will be necessary to connect the top of R4 to ground (position B).

Two frequency ranges are provided, which are selected by means of S1; 12 Hz-1 kHz and 1 kHz to about 70 kHz. Fine frequency control is provided by P1 which varies the charge and discharge current of C1 or C2 and hence the rate at which the integrator ramps up and down.

The squarewave output from N3 is taken via a waveform selector switch, S2, to a buffer amplifier, which consists of two inverters (connected in parallel to boost their output current capability) biased as a linear amplifier. The triangle output is taken through a buffer amplifier N4, and thence through the selector switch to the output buffer amplifier.

The triangle output from N4 is also taken to the sine shaper, which consists of R9, R11, C3, D1 and D2. Up to about plus or minus 0.5 volts D1 and D2 draw little current, but above this voltage their dynamic resistance falls and they limit the peaks and troughs of the triangle signal logarithmically to produce an approximation to a sinewave. The sine output is fed via C5 and R10 to the output amplifier.

Sine purity is adjusted by P4, which varies the gain of N4 and thus the amplitude of the triangle signal fed to the sine shaper. Too low a signal level, and the triangle amplitude will be below the diode threshold voltage, so that it will pass without alteration; too high a signal level, and the peaks and troughs will be clipped severely, thus not giving a good sine wave.

The input resistors to the output buffer amplifier are chosen so that all three waveforms have a peak to peak output voltage of about 1.2 V maximum. The output level can be adjusted by P3.

Adjustment procedure

The adjustment procedure consists simply of adjusting the triangle symmetry and sine purity.

Triangle symmetry is actually best adjusted by observing the squarewave signal, since a symmetrical triangle is obtained when the squarewave duty-cycle is 50% (1-1 mark-space ratio). P2 is adjusted to achieve this. In cases where the symmetry improves as the wiper of P2 is turned down towards the output of N3 but exact symmetry cannot be obtained, the top of R4 should be connected in the alternative position.
Sine purity is adjusted by varying P4 until the waveform 'looks right' or by adjusting for minimum distortion if a distortion meter is available. Since the supply voltage alters the output voltage of the various waveforms, and hence the sine purity, the circuit should be operated from a stable 6 V supply. If batteries are used they should never be allowed to run down too far.
CMOS ICs used as linear circuits draw more current than when used in the normal switching mode, and the supply voltage should not be greater than 6 V, otherwise the IC may overheat due to excessive power dissipation.

Performance

The quality of the waveforms can be judged from the oscilloscope photographs. In all three cases the vertical sensitivity is 500 mV/div and the timebase speed 200 μ s/div.

7 Zener tester

This simple tester provides a reliable means of measuring zener voltages and of plotting the variation of zener voltage with zener current.

In many cases the breakdown voltage of a zener diode is printed, fairly clearly, on the case. For example, the type number of the zener family is often printed, together with the zener voltage, so a BZY88 6V8 would be a 6.8 V zener from the BZY88 family. Unfortunately, some manufacturers merely print an indecipherable code, which has to be looked up in the relevant data book in order to find the zener parameters. Furthermore, there is sometimes a requirement for testing 'job lots' of unmarked devices, or components that have been lying in the junkbox and have had their markings rubbed off. In all these cases a zener tester can prove a useful addition to the 'lab' test equipment.
The reverse characteristic of a zener diode is illustrated in figure 1. At voltages below the zener voltage the device draws very little current. Once the breakdown voltage is reached any further increase in voltage will produce a large increase in current, i.e. above its breakdown voltage the zener diode behaves as a more or less constant voltage device. However, since the zener diode possesses a finite internal resistance (known as the dynamic resistance), the zener voltage will vary slightly with current, due to the voltage dropped across this internal resistance. Because of this, manufacturers always quote zener voltage at a certain current (usually between 5 and 10 mA).
It is, of course, possible to test a zener diode using a battery, series resistor and a multimeter to measure the zener voltage. However, the current flowing through the zener will be determined by the value of the resistor and the difference between the battery voltage and the zener voltage, and will obviously be less for high-voltage zeners than for low-voltage zeners. This can lead to errors in the measurement.
The zener tester described in this article feeds a known, constant current through the zener. Furthermore, a choice of seven different zener currents is provided, which allows the zener voltage to be plotted against current.
The circuit of the zener tester, which contains only nine components, is given in figure 2. T1 and T2 function as a voltage regulator. T1 receives a bias voltage from the supply via R4 and draws current from the supply through the zener under test. However, if the emitter voltage

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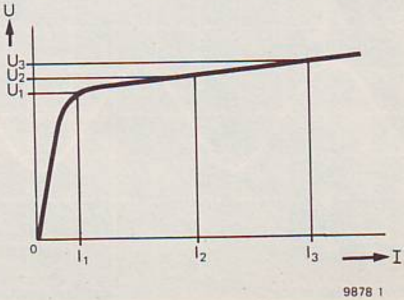

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should try to rise above the 0.6 V base emitter knee voltage of T2, then T2 will draw more current, pulling down the base voltage of T1 and thus reducing the emitter voltage. Should the emitter voltage of T1 tend to fall below the base-emitter voltage of T2, then T2 will draw less current, the collector voltage will rise, and with it the emitter voltage of T1. This negative feedback system means that a constant voltage of approximately 0.6 V appears at the emitter of T1.

If one or more of the switches S1 to S3 is closed, then a current $I = \frac{0.6}{\text{'R'}}$ (A, V, Ω) will flow

through one or more of the resistors R1-R3. ('R' is R1, R2, R3 or the parallel connection of two or more of these). This current will also flow through T1 and the zener. The zener voltage can then be measured by connecting a multimeter across it as shown. This should have a fairly high resistance (20,000 Ω /V or higher), so that it does not 'rob' too much current from the zener. By pressing one or more switches in different combinations a total of seven different zener currents can be obtained.

The zener currents for different combinations of the switches are shown in table 1. However, it should be noted that the actual currents obtained may vary by 10% from these figures, due to resistor tolerances and the temperature coefficient of T2.

The values of zener voltage obtained for different zener currents may be plotted on a graph of zener voltage versus zener current, as shown in figure 3. The dynamic resistance of the zener can then be calculated by dividing an increment in voltage, Δ U, by the corresponding increment in current, Δ I, i.e.

$$R_{dynamic} = \frac{\Delta U}{\Delta I}$$

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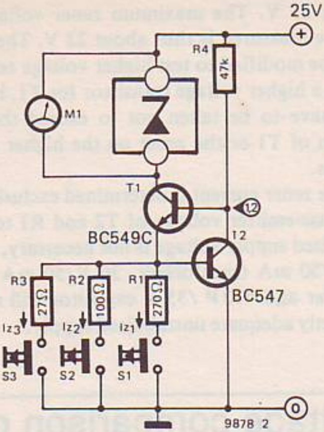

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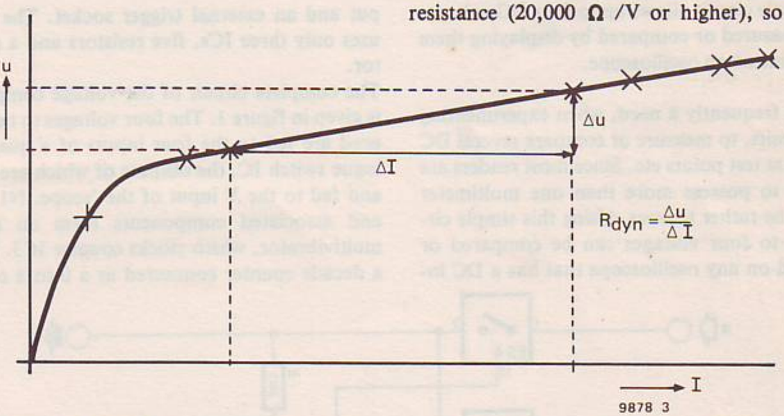

Figure 1. Voltage versus current characteristic of a zener diode. Even when the breakdown voltage has been reached, the zener voltage varies slightly with current.

Figure 2. Circuit of the zener tester. Pressing S1, S2 or S3 in various combinations feeds a choice of seven different constant currents through the zener and the zener voltage is measured with a multimeter.

Figure 3. A voltage versus current curve for the zener may be plotted, from which the dynamic resistance may be found.

Table 1. The theoretical currents for the various combinations of S1, S2 and S3. These may vary in practice by 10%, due to component tolerances.

Switch	U_b	I_Z
S1	25 V	2.22 mA
S2	25 V	6 mA
S3	25 V	22.2 mA
S1 + S2	25 V	8.2 mA
S1 + S3	25 V	24.4 mA
S2 + S3	25 V	28.2 mA
S1 + S2 + S3	25 V	30 mA

With the supply voltage shown, the maximum voltage that can appear between positive supply and the collector of T1 without T1 saturating is about 23 V. The maximum zener voltage that can be measured is thus about 22 V. The circuit may be modified to test higher voltage zeners by using a higher voltage transistor for T1, but care will have to be taken not to exceed the dissipation of T1 or the zener on the higher current ranges.

As the zener current is determined exclusively by the base-emitter voltage of T2 and R1 to R3, a stabilised supply voltage is not necessary, and an 18 V/50 mA transformer, 30 V/50 mA bridge rectifier and 470 µ /35 V capacitor will make a perfectly adequate unstabilised supply.

8 Voltage comparison on a 'scope

This simple circuit allows up to four DC voltages to be measured or compared by displaying them side by side on an oscilloscope.

There is frequently a need, when experimenting with circuits, to measure or compare several DC voltages at test points etc. Since most readers are unlikely to possess more than one multimeter this can be rather tedious. Using this simple circuit, up to four voltages can be compared or measured on any oscilloscope that has a DC input and an external trigger socket. The circuit uses only three ICs, five resistors and a capacitor.

The complete circuit of the voltage comparator is given in figure 1. The four voltages to be measured are fed to the four inputs of a quad analogue switch IC, the outputs of which are linked and fed to the Y input of the 'scope. N1 to N3 and associated components form an astable multivibrator, which clocks counter IC3. This is a decade counter connected as a 0 to 3 counter

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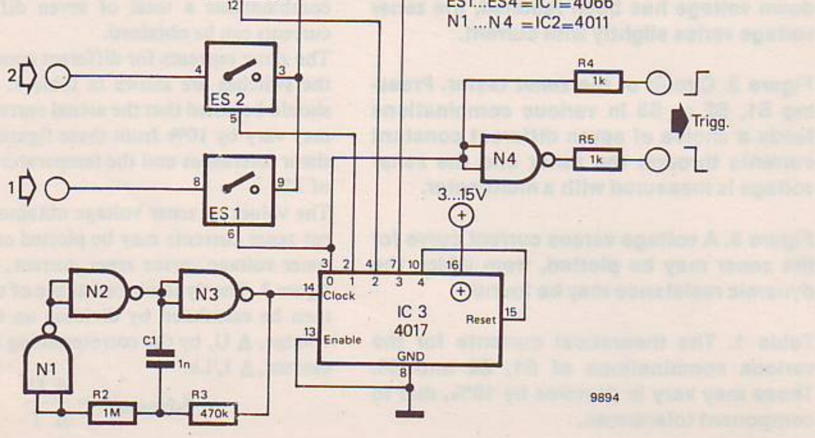
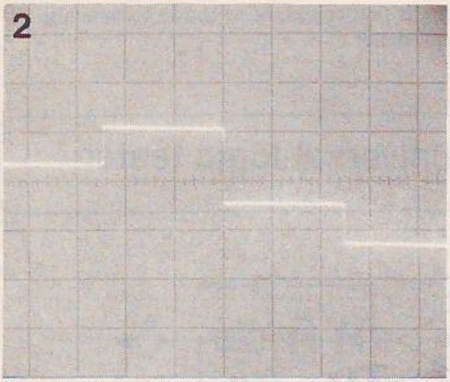


Figure 1. The circuit diagram of the voltage comparator.

Figure 2. An example of 4 random voltage levels displayed simultaneously on the 'scope.



by feedback from output 4 to the reset input. Outputs 0 to 3 of the counter go high in turn, thus 'closing' each of the analogue switches in turn and feeding the input voltages to the 'scope in sequence.
Output 0 of the counter feeds a trigger pulse to the 'scope once every four clock pulses, so that for every cycle of the counter the 'scope trace makes one sweep of the screen. A positive-going trigger pulse is available via R4, or a negative-going trigger pulse is available from the output of N4 via R5. The resulting display is shown in figure 2, four different input voltages being fed to the inputs in this case. The oscilloscope time-base speed should be adjusted so that the display of the four voltage levels just occupies the whole screen width.
The supply voltage $+U_b$ may be from 3 to 15 V, but it must be noted that the input voltage should be positive with respect to the 0 V rail and not greater than $+U_b$. If voltages greater than this are to be measured then potential dividers must be used on the four inputs.

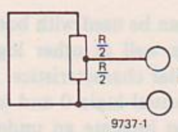
Setting up

To calibrate the circuit, simply feed a known voltage into one input and adjust the Y sensitivity of the 'scope to give a convenient deflection (for example one graticule division per volt input). The unknown voltages may then be fed in and compared against each other and against the calibration.
The circuit can easily be extended to eight inputs by adding an extra 4066 IC and connecting IC3 as a 0 to 7 counter (reset connected to output 8, pin 9).

H. Spenn

9 Real load resistors

When measuring and comparing the output powers of audio amplifiers (especially at the high end of the audio spectrum) it is useful to have available a 'real' load resistor, i.e. one which is a pure resistance with no parasitic inductance or capacitance. Carbon film resistors have a low self-inductance, but unfortunately are not commonly available in the high power ratings required for amplifier testing. The highest rating normally available in a carbon film resistor is 2 watts, so a load resistor for testing a 100 W amplifier would need to be made up of 50 such resistors in series/parallel combinations!
Wirewound resistors are available with high power ratings, but unfortunately such resistors are rarely wound so as to minimise self-inductance. A typical high-power wirewound resistor consists of a single layer of resistance wire



wound helically on a cylindrical ceramic tube. This type of resistor has quite a high self-inductance, but since the usual applications of high-power wirewound resistors are DC or low-frequency AC this is not important.
For use as an amplifier load resistor some means must be found of reducing the inductance of a wirewound resistor. This can be achieved by providing the resistor with a centre tap and connecting it as shown in figure 1. Current flows in opposite directions in each half of the resistor, so the magnetic fields produced in each half (and hence the self-inductances) tend to cancel out. If

the original resistor has a value R then the connection shown has a resistance R/4 since it consists of two R/2 sections in parallel.
Resistors already provided with taps, such as television H.T. dropper resistors, are suitable for this application. Presettable resistors may also be used. These consist of an exposed wire element wound on a ceramic former, and are provided with contact clips that may be fixed anywhere along the length of the element. 1 kW electric fire (heating) elements (which have a resistance of around 60 Ω) may also be used.
In order to obtain a load resistor of the desired resistance and wattage rating, several wirewound resistors may be connected in series/parallel combinations in the normal way, provided each one is first connected as shown to minimise its inductance.

10 Universal logic tester

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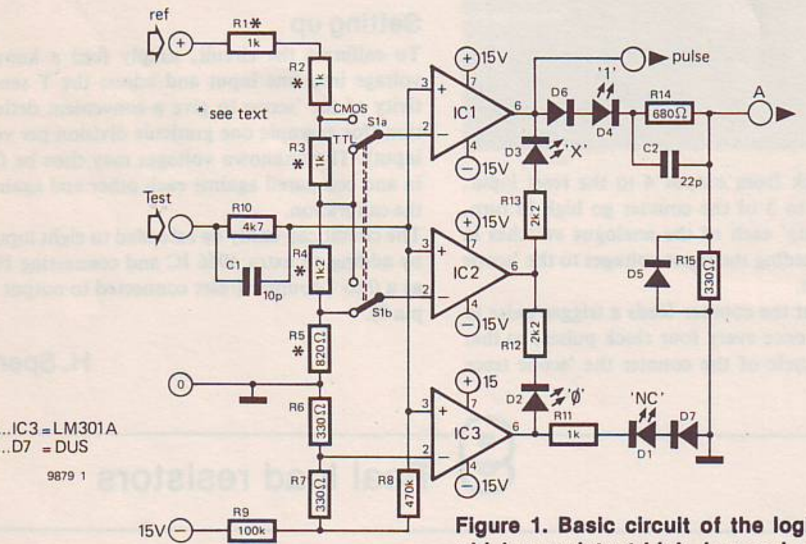

Figure 1. Basic circuit of the logic tester, which can detect high, low and undefined logic levels, and open-circuits.

Figure 2. A 'pulse stretcher' monostable.

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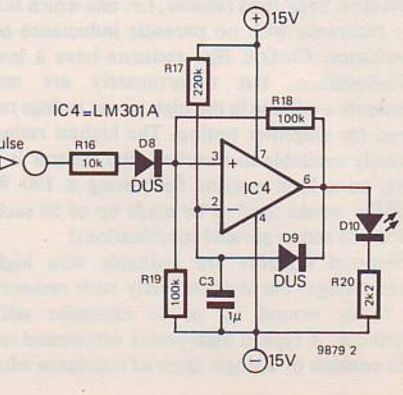


This logic tester can be used with both TTL and CMOS circuits as well as other logic families which exhibit similar characteristics. In addition to providing the usual logic 0 and logic 1 indications it will also indicate an undefined logic level and open circuit connections.

In TTL circuits a voltage less than 0.8 V is defined as logic 0 or 'low', and a voltage greater than 2 V is defined as logic 1 or 'high'. A voltage between these two is referred to as an undefined logic level. CMOS logic is capable of operating over a much wider supply range than TTL, typically 3 - 18 V. The logic levels for CMOS are not defined as absolute voltages but as percentages of supply voltage. A high logic level is defined as greater than 60% of supply voltage, and a low level is defined as less than 40% of supply volt-

age. Levels between these limits are undefined.
A logic probe must be capable of distinguishing between low, high and undefined logic levels. There is also the possibility that an open-circuit may be encountered when using a logic tester. This could be due to the test probe not making good contact; or due to a circuit fault. Also, sometimes pins are intentionally not connected to anything (known as NC or No Connection in manufacturers' data). A logic tester must be capable of distinguishing an open-circuit from any of the other logic levels.
The circuit of the logic tester is shown in figure 1. Three voltage comparators are used to detect the four possible input conditions. The 'ref +' (reference) and '0' terminals of the tester are connected to the supply lines of the logic circuit under test. With a 5 V supply and S1 set to the 'TTL' position, 2 V will be present at the inverting input of IC1 and 0.8 V at the inverting input of IC2. With S1 set to the CMOS position the reference voltages will be respectively 60% and 40% of the supply voltage of the circuit being tested.
The inverting input of IC3 receives a potential of about −50 mV via R9, R7 and R6 from the negative rail of the tester's own (± 15 V) supply. When the 'test' input is open-circuit, the non-inverting inputs of the three comparators will be pulled down to about −100 mV via R8. The outputs of all three comparators will be negative, so LED D1 will be lit. If the test input is connected to a voltage between zero volts and the logic 0 level the output of comparator IC3 will swing positive and D2 will light due to current flowing through it from the output of IC3 into the output of IC2, thus indicating 'logic 0'.
For voltages between the logic 0 and logic 1 levels the output of IC2 will also swing positive. D2 will extinguish and D3 will light due to current flowing through it from the output of IC2 to the output of IC1. This LED indicates the undefined logic state 'X'. When the logic 1 threshold is exceeded the output of IC1 will swing positive. D3 will extinguish and D4 will light, thus indicating 'logic 1'.

Pulse indication

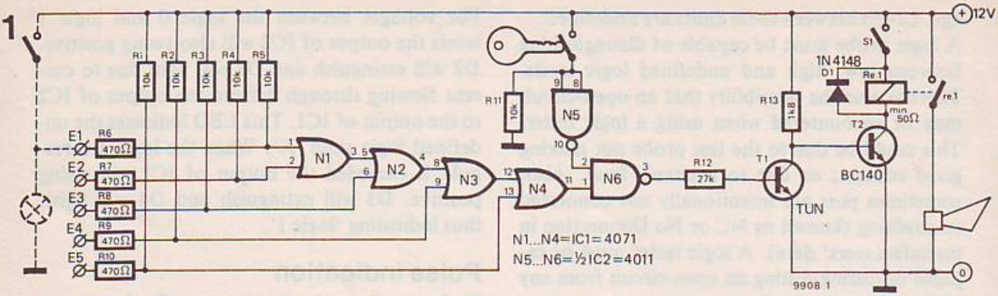
So far the discussion has been confined to the indication of static logic levels. However, pulses and pulse trains are frequently encountered in logic circuits. Pulse trains with a duty-cycle near 50% will cause both D2 and D4 to glow with reduced brightness. However, if the duty-cycle of a pulse train is very large or very small it will appear that one LED is lit continuously.
Also, short single pulses will be missed completely. To overcome this problem a 'pulse stretcher' circuit may be used, see figure 2.
The pulse stretcher is a one-shot multivibrator with an output pulse period of approximately 200 ms. When any pulse appears at the point in figure 1 labled 'pulse', which is connected to the input of the pulse stretcher, the one-shot will be triggered and the LED will glow for about 200 ms. This is sufficiently long for the indication to be seen. If the pulse rate is greater than 5 Hz, D10 will appear to glow continuously.
A TTL-compatible pulse output is provided (A) for simple frequency counters etc. If this is not required, C2 and D5 can be omitted and R14 and R15 are replaced by a single 1 k resistor.

J. Borgman

11 Car rip-off protection

Thefts from cars of valuable accessories such as spotlamps and foglamps are on the increase. Equipped with a spanner, and given a few minutes undisturbed, the enterprising felon can frequently make a haul worth over £100. The inexpensive alarm circuit described here will protect these valuable items, and can also be used to prevent the theft of accessories from inside the car, for example radios and cassette players.

The complete circuit of the alarm is shown in figure 1. N1 to N4 form a 5-input OR gate, but the number of inputs can easily be increased by adding extra gates. When the car is unoccupied (and the ignition is switched off) R11 holds the inputs of N5 low, so the output is high. The inputs of N1 to N4 are held low via the filaments of the lamps, etc. that are being protected. The output of N4 is thus low, the output of N6 is high, T1 is turned on, T2 is turned off and relay Re.1 is de-



energised.

In the event of an accessory being disconnected by a thief (for example, the lamp connected to input E1), then the appropriate input to the OR gate will be pulled high by the 10 k input resistor. The output of N4 then goes high, the output of N6 goes low, T1 is turned off and T2 is turned on, energising Re.1 and sounding the car horn.

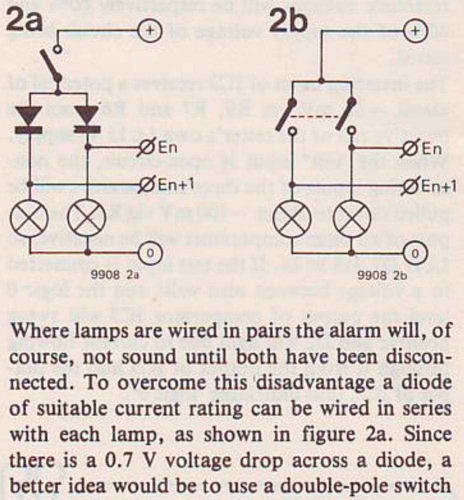
When the ignition switch is closed the output of N5 is low, which holds the output of N6 permanently high, thus disabling the alarm. This prevents the alarm from sounding when one of the accessories is switched on. Of course, the alarm will still sound if an accessory is switched on whilst the ignition is switched off. This prevents spotlamps and foglamps from accidentally being left on whilst the car is unoccupied. Alternatively, these accessories can be wired via the ignition switch so that this cannot occur.

An additional bonus is that the alarm will also sound in the event of a lamp filament failure. However, since a replacement lamp may not always be available, a secret 'cancel' switch (S1) is required...

Accessories inside the car, such as radios and cassette players, may also be protected by connecting a wire from one of the alarm inputs to the earthed case of the equipment. When the thief cuts this wire to remove the equipment then the alarm will sound. Of course, this facility should only be regarded as a backup to an alarm that prevents a thief entering the car in the first place!

Figure 1. Complete circuit of the car rip-off theft alarm.

Figure 2. Lamps connected in pairs must be isolated from one another, otherwise the alarm will not give complete protection. This can be done with a pair of diodes, as shown in figure 2a, or by double-pole switching, as shown in figure 2b.



Where lamps are wired in pairs the alarm will, of course, not sound until both have been disconnected. To overcome this disadvantage a diode of suitable current rating can be wired in series with each lamp, as shown in figure 2a. Since there is a 0.7 V voltage drop across a diode, a better idea would be to use a double-pole switch for the set of lamps being protected, as shown in figure 2b.

W. Braun

12 Automatic mono stereo switch

For some time now owners of stereo FM receivers will have noticed that the stereo indicator lamp stays on continuously. This is due to a decision by the BBC to transmit the 19 kHz pilot tone with all programmes, ostensibly to eliminate annoying clicks that occur when switching

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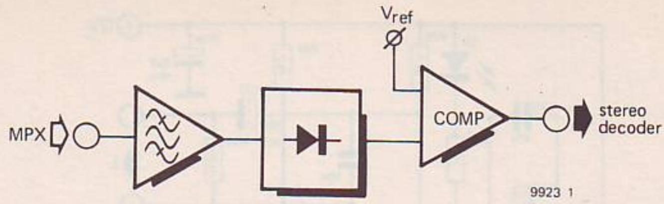

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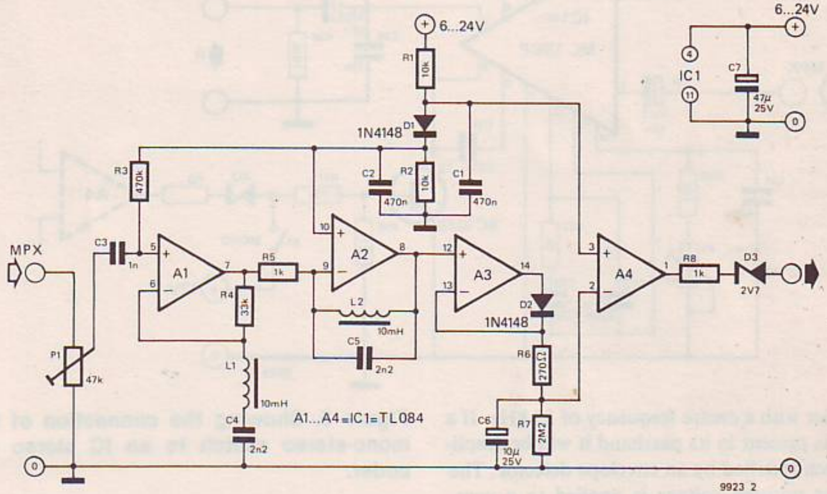

the pilot tone on and off. The commercial radio stations have, of course, followed this practice for some time.

As the mono-stereo switch in a stereo receiver operates by detecting the pilot tone, this means that such receivers are now incapable of distinguishing between mono and stereo transmissions and will be permanently switched to stereo unless the 'mono' switch is pressed. Apart from the minor annoyance of not knowing if a programme is in stereo (unless one buys the Radio Times) there is the greater inconvenience of listening to mono transmissions with the poorer signal-to-noise ratio inherent in stereo transmission. This is particularly a problem in areas of fringe reception. The circuit described in this article distinguishes between mono and stereo transmissions by detecting whether or not stereo information is present in the received signal, independent of the pilot tone.

When an FM stereo transmission has been demodulated, but before it has been decoded, it consists of two distinct channels. The left plus right (L + R) signal occupies the frequency band 0...15 kHz. This signal is essential for mono compatibility, as it is the only part of the stereo signal that a mono radio can receive. The frequency band from 23...38 kHz is occupied by the lower sideband of a 38 kHz subcarrier, onto which the L – R (left minus right) signal is modulated. In principle the stereo signal is decoded by demodulating this signal, adding it to the L + R signal to get 2L, and subtracting it from the L + R signal to get 2R. Since the 23...38 kHz signal is absent during a mono transmission, a circuit which can detect this signal will be able to distinguish between mono and stereo transmissions. This is the principle of the automatic mono-stereo switch.

Figure 1. Block diagram of the automatic mono-stereo switch.

Figure 2. Complete circuit of the mono-stereo switch.

Block diagram

The principle of the automatic mono-stereo switch is illustrated in the block diagram of figure 1. A portion of the signal from the output of the detector stage of the tuner is fed to a selective

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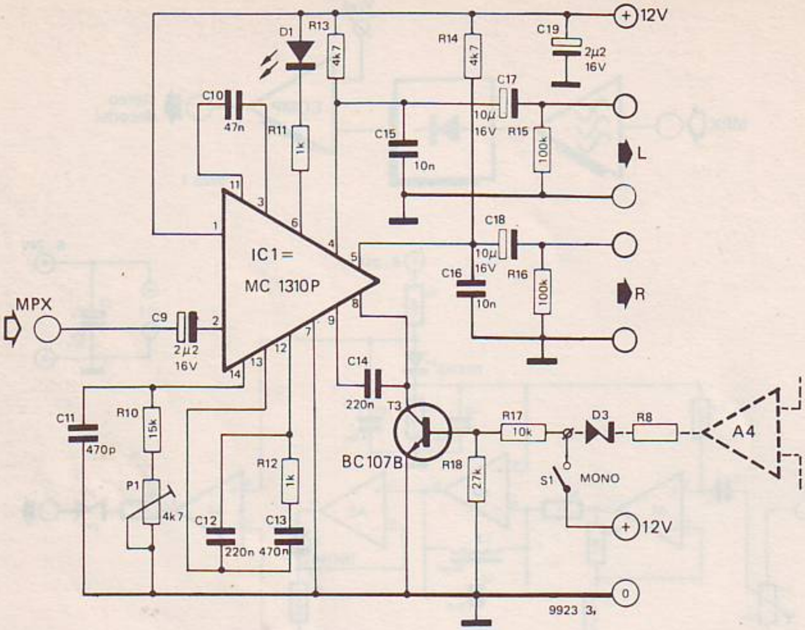

amplifier with a centre frequency of 35 kHz. If a signal is present in its passband it will be amplified, then rectified by an envelope detector. The resulting positive voltage is applied to a comparator, whose output swings negative and switches on the stereo decoder. If the transmission is mono then no signal will be fed through the selective amplifier and the comparator output will remain high, switching off the stereo decoder.

Complete circuit

The circuit of the mono-stereo switch is shown in figure 2. A1 to A4 are the four sections of a TL084 quad FET opamp. The selective amplifier is built around A1 and A2, the passband being determined by L1, L2, C4 and C5. A positive bias voltage of just less than half supply voltage is applied to the selective amplifier from the junction of R2 and D1. This is fed through the rectifier A3 to appear on capacitor C6 and hence at the inverting input of comparator A4. The non-inverting input of A4 receives a positive bias slightly higher than half supply voltage from the junction of R1 and D1. Under no-signal conditions the output of A4 is therefore positive. The output signal of the tuner is fed to the input of A1 via sensitivity control P1 and C3. If stereo information is present this will be amplified by A1 and A2 and rectified by A3, causing the voltage on C6 to rise above that at the non-inverting input of A4. The output of A4 will thus swing down to 0 V, turning on the stereo decoder.

The attack time of the rectifier is extremely short, about 2.7 ms, so the decoder will be switched to stereo immediately a stereo signal is received. However, to avoid the decoder switching back to mono during pauses in the audio signal, the decay time constant R7-C6, is made fairly long, and the circuit will not switch back to mono operation until about 20 seconds after the cessation of a stereo signal.

The mono-stereo switch can be connected to most IC stereo decoders, such as the MC1310P, as shown in figure 3. Operation of the manual mono switch which allows selection of mono operation if stereo reception is too noisy, is unaffected.

Figure 3. Showing the connection of the mono-stereo switch to an IC stereo decoder.

Figure 4. A suggested printed circuit board design and component layout for the circuit of figure 2.

Construction

A printed circuit board and component layout

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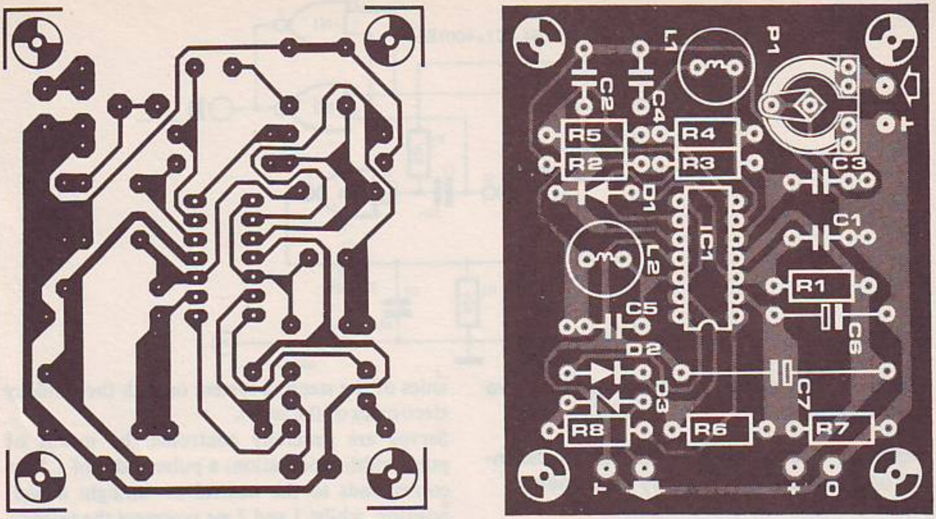


Parts list for figures 2 and 4

Resistors:
R1, R2 = 10 k
R3 = 470 k
R4 = 33 k
R5 = 1 k
R6 = 270 Ω
R7 = 2M2
R8 = 1 k

Capacitors:
C1, C2 = 470 n
C3 = 1 n
C4, C5 = 2n2
C6 = 10 µ /25 V
C7 = 47 µ /25 V

Semiconductors:
IC1 = TL 084
D1, D2 = 1N4148
D3 = zener 2V7

Miscellaneous:
P1 = 47 k preset
L1, L2 = 10 mH choke

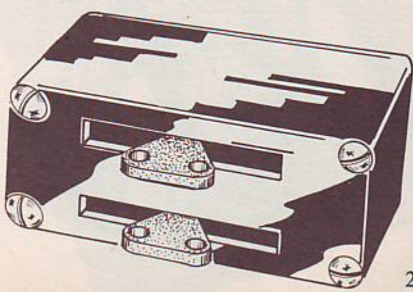
for the mono-stereo switch are given in figure 4. This p.c.b. should be sufficiently compact to be built into most FM tuners, and the wide supply voltage range should allow the circuit to be powered from the supply rail of almost any tuner.

The circuit has only one adjustment, the sensitivity control P1. This should be adjusted so that the circuit operates on any stereo signal which is sufficiently strong for noise-free stereo listening. On the other hand, the sensitivity of the circuit must not be so great that it switches on spurious noise.

13 Servo polarity changer

Many model enthusiasts will be familiar with situations in which they discovered that moving a servo control in one direction prompted the model to steer in the opposite direction! The circuit described here is intended to offer a simple solution to just this problem.

The best results are usually obtained from a servo mechanism if it is mounted in the model so there are as few joints and bends in the steering rod as possible. However the direction in which the servo moves should be such that it coincides with the direction of the control knob or joystick, i.e. moving the joystick to the right causes the model to steer to the right. However, in certain cases these two conditions prove mutually incompatible. Often the result is that the model builder has to tamper with the delicate mech-



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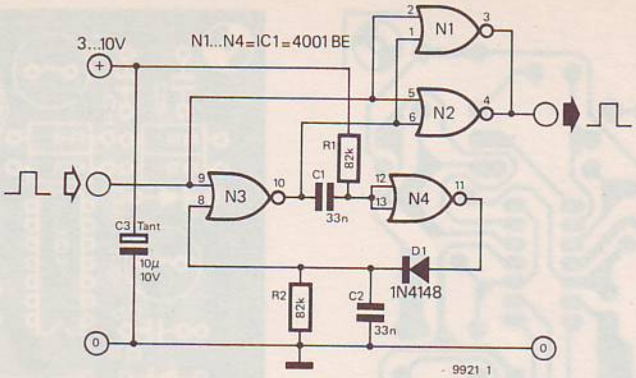

Figure 1. The circuit diagram of the servo polarity changer.

Figure 2. The finished circuit when mounted on a board occupies very little space.

Figure 3. In order to set the servo in the neutral position a pulse duration of 1.5 ms is required. The top channel shows the input signal of the circuit, whilst the bottom channel shows the output pulse. The pulse is shifted along the time axis, but this has no effect upon the operation of the servo.

Figure 4. This photo shows the output pulse obtained for an input pulse duration of 1 ms. As is apparent the duration of the output pulse is 2 ms, so that the servo will now be moved exactly the same amount (the distance corresponding to a pulse of 0.5 ms) as in the pulse of the input signal, but in the opposite direction.

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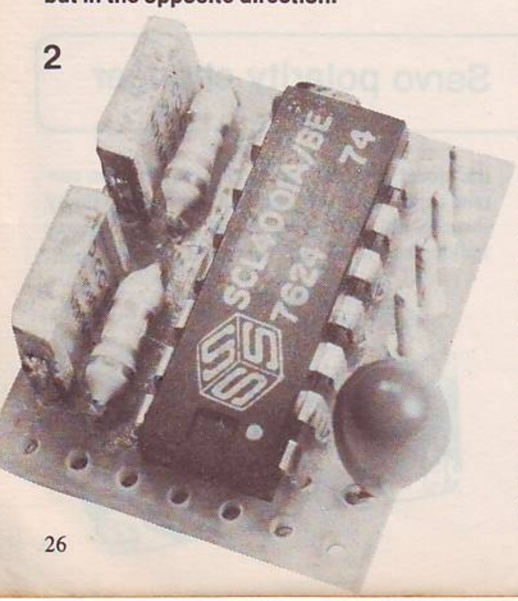

anics of the steering system or with the finnicky electronics of the servo.

Servos are generally controlled by means of pulse width modulation; a pulse width of 1.5 ms corresponds to the neutral or 'straight ahead' position, whilst 1 and 2 ms represent the extreme settings of the control. The polarity of a servo can simply be reversed, so that a pulse width of 1 ms causes the servo control to assume the position that was previously adopted with a pulse width of 2 ms, and vice versa, by modifying the width of the control pulses.

Since in both cases the neutral position of the control will correspond to a pulse width of 1.5 ms, it is possible to calculate the pulse width for all other positions on the basis of this figure. This can be done quite simply by subtracting the original pulse width from 3 ms in order to obtain its counterpart in the opposite direction. Thus in order to reverse the polarity of the servo one simply arranges for the control pulses to be subtracted from a reference pulse of 3 ms.

There are two different types of servo which are currently available, namely those which operate with positive going control pulses, and those which require a negative going pulse. The circuit described here can only be used with servos which use positive going pulses, however this represents the large majority of commercially available devices. The finished circuit occupies very little space (see figure 2) and hence there should be no problems mounting it in whatever model is under construction.

The circuit

N3 and N4 along with C1, C2, R1, R2 and D1 form a monostable with a pulse duration of approx. 3 ms. This monostable is triggered by the control signal, which is also fed to one of the inputs of N1 and N2. The other inputs of these two gates receive negative going pulses of approx. 3

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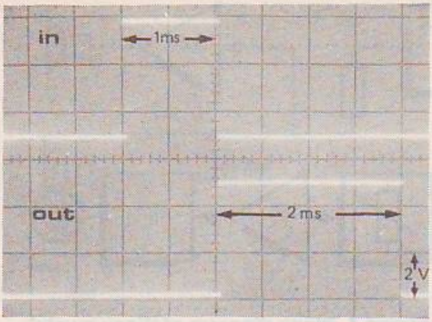

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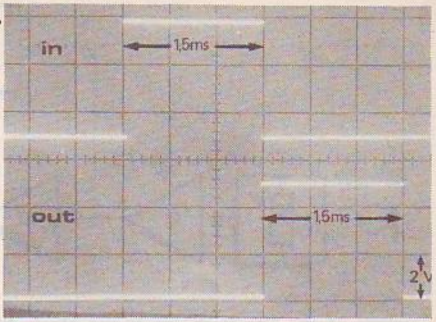

ms duration from the output of N3. Since N1 and N2 (like N3 and N4) are NOR gates, their output will produce a positive going pulse, the duration of which is equal to the difference between 3 ms and the original control pulse. N2 is connected in parallel with N1 to increase the fan-out of the circuit.
The oscilloscope photos show the result before and after a pulse has been processed by the circuit. In the prototype model the duration of the monostable pulse was 3.15 ms. In most applications where the servo is permanently built into the model, allowance for slight tolerances in pulse width can be made at the transmitter. However, if a pulse duration of exactly 3 ms is required, then a value of 27 n should be chosen for C1 and C2. Smaller capacitors can then be connected in parallel with these until a pulse of precisely 3 ms is obtained on the scope. Without a scope the pulse width can still be accurately set by altering the value of C1 and C2 in the above fashion until, with or without the polarity changer, the servo remains in exactly the neutral position.
The circuit consumes very little current (1 mA), and is unaffected ($< 2\%$) by variations in the supply voltage between 3 and 10 V. In order to reduce the dimensions of the circuit to a minimum, a tantalum type is recommended for C3. As a result of the symmetrical construction (R1 = R2, C1 = C2) the circuit has a very low temperature coefficient.

14 Easy music

For those who do not have the time (or perhaps the patience) to master a musical instrument, but would nonetheless like to make their own music, this simple circuit may provide the answer. The only musical accomplishment necessary is the ability to whistle in tune.

The principle of 'Easy music' is extremely simple, as can be seen from the block diagram of figure 1. The 'musician's' whistle is picked up by a crystal microphone and amplified by opamp A1. A portion of the signal is fed to an envelope follower, which rectifies and filters it to produce a positive voltage that follows the amplitude envelope of the input signal. The signal is also fed to two limiting amplifiers, which convert the variable amplitude sinewave of the input signal into a constant amplitude squarewave having the same frequency as the input signal. This squarewave is used to clock a binary counter whose division ratio can be set to 2, 4, 8 etc., so that the output is one, two, three etc. octaves below the input signal.
The counter output is used to switch transistor T1 on and off, and the collector signal of T1 is fed to the output amplifier A4. Since the collector resistor of T1 receives its supply from the output of the envelope follower, the amplitude of the collector signal, and hence of the output signal, varies in sympathy with the amplitude of the original input signal.
The output is therefore a squarewave whose frequency may be one or more octaves lower than the input signal and whose amplitude dynamics follow the amplitude of the input signal.

Complete circuit

The complete circuit is given in figure 2, and the

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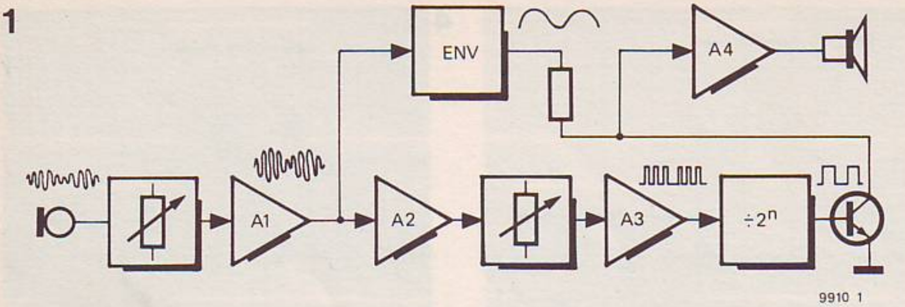

sections of the circuit shown in the block diagram are easily identified. The output of the crystal microphone is fed to P1, which functions as a sensitivity control. A1 is connected as a linear amplifier with a gain of approximately 56. A portion of the output signal from A1 is rectified by D1 and the resulting peak positive voltage is stored on C4. The output signal from A1 is further amplified by A2 and A3, the combined gain of A1 to A3 being sufficient to cause limiting at the output of A3, even with very small input signals. P2 is used to adjust the gain of the limiting amplifier so that limiting just occurs with the smallest input signal, this avoiding limiting caused by extraneous noises.

The output of A3 is used to clock a CMOS binary counter, whose division ratio may be set by means of S1. The output of IC2 switches transistor T1 on and off. Since the collector resistor of T1 (R6) receives its supply voltage from C4, the amplitude of the collector signal varies in sympathy with the input signal. This signal is amplified by a small audio power amplifier built around A4, which drives a small loudspeaker.

Figure 1. Block diagram of 'Easy music'.

Figure 2. Complete circuit diagram.

Additions to the basic circuit

However, the possibilities do not end there. The more ambitious constructor may wish to add filters and other circuits to produce different output waveforms which will extend the tonal possibilities of the instrument. Such variations on the basic design are, however, beyond the scope of this short article, and are left to the ingenuity of the individual reader.

P.J. Tyrrell

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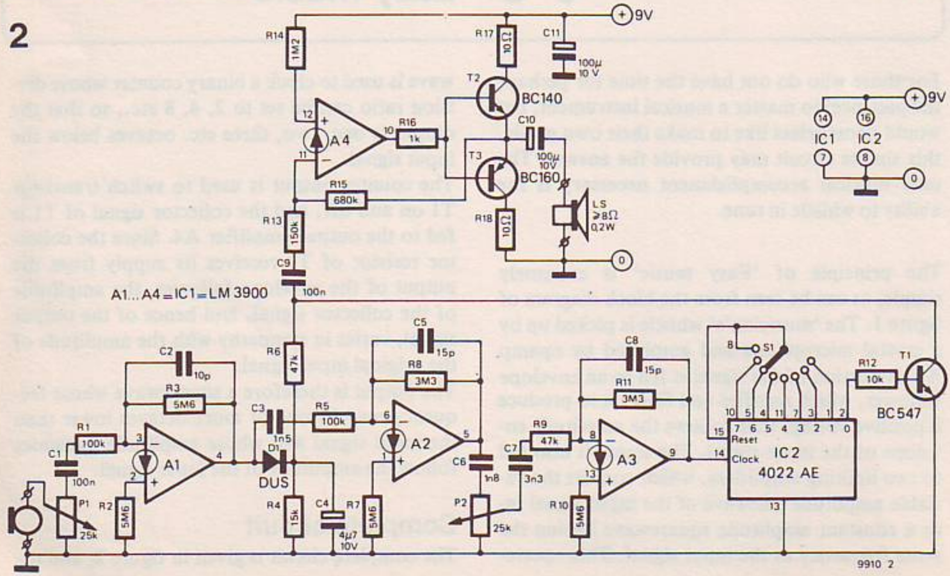

15 duty-cycles at the turn of a switch

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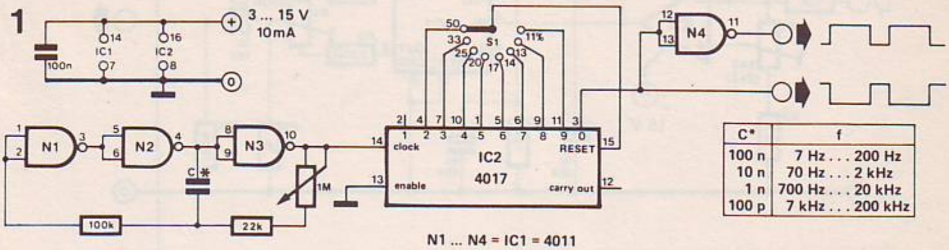

C*	f
100 n	7 Hz . . . 200 Hz
10 n	70 Hz . . . 2 kHz
1 n	700 Hz . . . 20 kHz
100 p	7 kHz . . . 200 kHz

Figure 1. Only two IC's are required for this little generator. The Table lists frequency ranges for a few capacitor values.

Figure 2. The duty-cycle at the output is determined by the division ratio.

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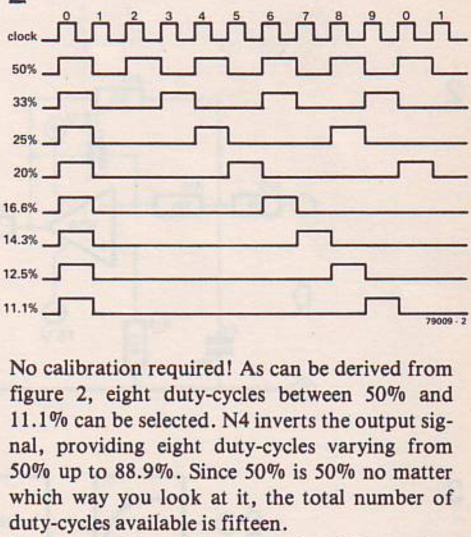

Only two CMOS-ICs are used in the generator described here, but in spite of its simplicity it offers a selection of 15 precisely determined duty-cycles without any need for calibration. It is a useful item of test gear, especially for calibrating other instruments that are designed to measure duty-cycles in one form or another – dwell meters, for instance.

The outputs of a divide-by-ten counter, the CD4017, are connected to an 8-position switch. One of the outputs is selected and fed back to the reset input of the IC. The result is a divider stage that can be set at any division ratio between 2 and 9. If the output is taken from the '0' output of the divider, both the frequency and the duty-cycle of the input frequency will be 'divided' by the preset ratio. Furthermore, the duty-cycle of the output signal will be independent of the input frequency: it is determined only by the setting of the selector switch.

To complete the unit, a clock generator is included (N1...N3). The 'clock' frequency is determined by the value of the capacitor, C, and by the setting of the 1 M potentiometer. The Table lists frequency ranges for a few capacitor values. The duty-cycle at the output (pin 3 of IC2) is equal to the division ratio times 100%. For instance, if output '5' (pin 1) of IC2 is selected, the division ratio is 1:5 and the duty-cycle is

$$\frac{100}{5} = 20\%.$$

No calibration required! As can be derived from figure 2, eight duty-cycles between 50% and 11.1% can be selected. N4 inverts the output signal, providing eight duty-cycles varying from 50% up to 88.9%. Since 50% is 50% no matter which way you look at it, the total number of duty-cycles available is fifteen.

The amplitude of the output signal is equal to the supply voltage, i.e. anywhere between 3 and 15 volts.

16 Analogue delay line

There are numerous applications requiring the use of an audio delay line, for example phasing and vibrato units, echo and reverberation units, and sophisticated loudspeakers with active time-

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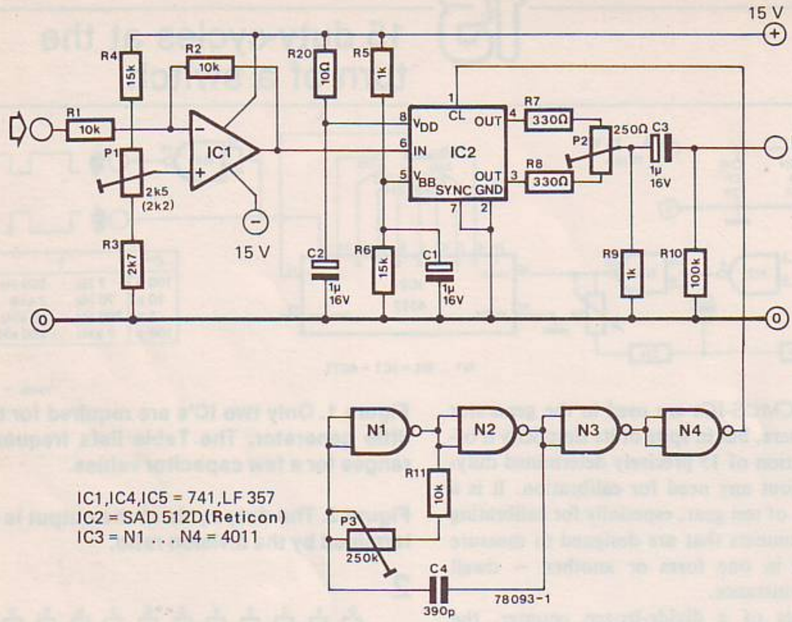

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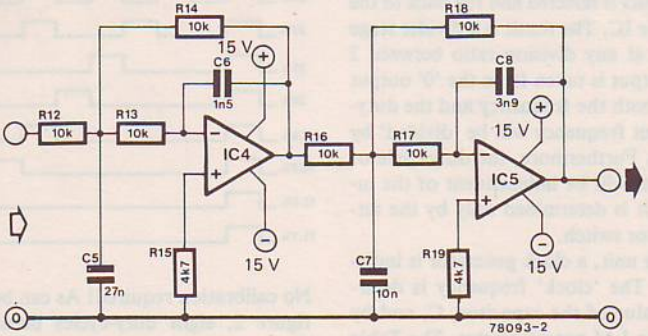

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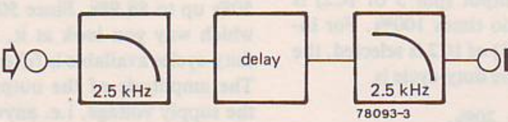


delay compensation. One of the simplest ways to achieve this electronically is to use an analogue (bucket brigade) shift register. There are various types on the market and a particularly interesting one is the Reticon SAD 512, which has 512 stages and a built-in clock buffer. The clock buffer enables it to be driven from a simple, single-phase clock circuit such as a CMOS multivibrator.

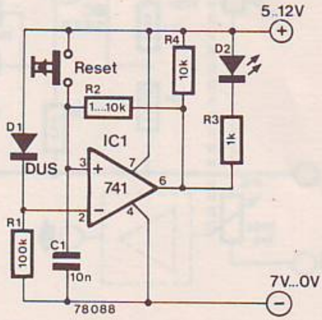
Figure 1 shows a delay line utilising the SAD 512. Input signals to the device must be positive with respect to the 0 V pin, so the AF input signal is first fed to an inverting amplifier, IC2, which has a positive DC offset adjustable by P1. The clock generator is an astable multivibrator using CMOS NAND gates (N1 and N2) and its frequency may be varied between 10 kHz and 100 kHz by means of P3. The clock buffer of the

SAD 512 divides the clock input frequency by two, so the sampling frequency, f_c, of the SAD512, varies between 5 kHz and 50 kHz. The delay produced by the circuit is $n/2f_c$, where n is the number of stages in the IC. The delay may therefore be varied between 5.12 ms and 51.2 ms. To obtain longer delays several SAD 512s may, of course, be cascaded very easily, since no special clock drive circuit is required.
To minimise clock noise the outputs from the final and penultimate stages of the IC are summed by R7, R8 and P2. However, if the circuit is to be used with the minimum clock frequency then clock noise will still be audible, and the lowpass filter circuit shown in figure 2 should be connected to the output. This consists of a fourth-order Butterworth filter with a turnover frequency of 2.5 kHz and an ultimate slope of -24 dB/octave.

Of course, if low clock frequencies are to be employed then the maximum frequency of the input signal must be restricted to half the sampling frequency. This can be achieved by connecting the filter circuit of figure 2 at the input of the delay line, as shown in figure 3.
To set up the circuit the clock frequency is lowered until it becomes audible. P2 is then adjusted until clock noise is at a minimum. The clock frequency is then raised and a signal fed in. The signal level is increased until distortion becomes apparent, whereupon P1 is adjusted to minimise distortion. This procedure (increasing the signal level and adjusting P1) is repeated until no further improvement is obtained. Alternatively, if an oscilloscope is available, P1 may be adjusted so that the waveform clips symmetrically when the circuit is overloaded by a large signal.

17 Supply failure indicator

Many circuits, especially digital systems such as random access memories and digital clocks, must have a continuous power supply to ensure correct operation. If the supply to a RAM is interrupted then the stored information is lost, as is the time in the case of a digital clock.
The supply failure indicator described here will sense the interruption of the power supply and will light a LED when the supply is restored, thus informing the microprocessor user that the information stored in RAM is garbage and must be re-entered, and telling the digital clock owner that his clock must be reset to the correct time.
When the supply is initially switched on the inverting input of IC1 is held at 0.6 V below positive supply by D1. Pressing the reset button takes the non-inverting input of IC1 to positive supply potential, so the output of IC1 swings high, holding the non-inverting input high even when the reset button is released. LED D2 is therefore not lit.



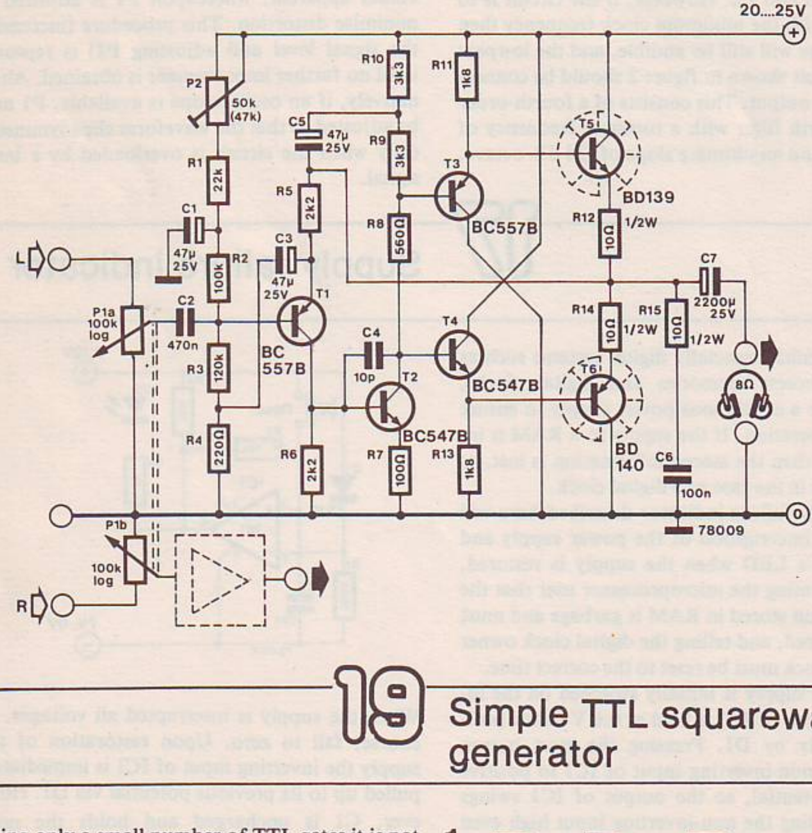
When the supply is interrupted all voltages, of course, fall to zero. Upon restoration of the supply the inverting input of IC1 is immediately pulled up to its previous potential via D1. However, C1 is uncharged and holds the non-inverting input low, so the output of IC1 remains low and D2 lights.

18 Amplifier for low-Z headphones

Stereo headphones are usually connected to the loudspeaker outputs of the power amp via an attenuator. Although this represents the cheapest solution, it does suffer from two

significant drawbacks: if the loudspeakers are also switched on whilst the headphones are being used, it is impossible to vary the signal level of the headphones independently of the loudspeakers; secondly, as a result of the output impedance of the attenuator, the damping factor of the system is reduced, which adversely affects the bass reproduction of the headphones. These problems can be solved however, by using this stereo output amp, which is connected via a stereo potentiometer (P1, P1′) to the tape output of the power amp. The tone controls will then have no effect upon the headphones, but in the case of better quality 'phones that is hardly an inconvenience.

The amplifier has an output power in excess of 1 Watt. The gain, which is determined by R4 and R5, is 11 (this can be varied, if so desired, by altering the value of R4). By means of P2 the voltage at the junction of R12 and R14 is adjusted to half supply. The quiescent current is 50 to 100 mA; this can be varied by altering R8.



19 Simple TTL squarewave generator

Using only a small number of TTL gates it is not difficult to construct a squarewave generator which can be used in a wide range of possible applications (e.g. as clock generator). The accompanying diagram represents the basic universal design for such a generator. The circuit is not critical, can be used over a wide range of frequencies, has no starting problems and is sufficiently stable for most applications. The frequency in not affected by supply voltage variations.

The oscillator frequency is determined by the RC

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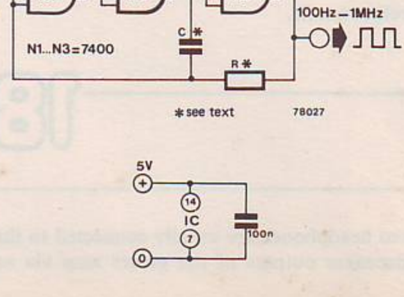

network and the propagation time of the inverters (in this case three NANDs with their inputs connected in parallel). Since the propagation delay time of the IC is, in general, strongly influenced by the temperature and supply voltage, care must be taken to ensure that the propagation times have as little effect as possible upon the oscillator frequency. The output of each gate changes state twice per period of the oscillation signal, which means that, in all, one must account for double the propagation time of all three gates. To ensure that the oscillator frequency f_o be more or less independent of variations in the temperature of the circuit and in the supply voltage, one must ensure that f_o is small compared to

$$\frac{1}{2 \cdot t_p \cdot n},$$

where t_p is the propagation time and n the number of inverters connected in series. In the case of the circuit shown here, t_p = approx. 10 ns and n = 3, so that as far as the oscillator frequency f_o is concerned:

$$f_o \ll \frac{1}{2 \cdot t_p \cdot n} = \frac{1}{2 \cdot 10 \cdot 3} = 16.6 \text{ MHz}.$$

The accompanying nomogram shows how f_o changes with R. The value of the resistor R must not be smaller than that shown in the nomogram; for example, for C = 100 nF, R must not be less than 100 Ω. A variable squarewave oscillator can be obtained by

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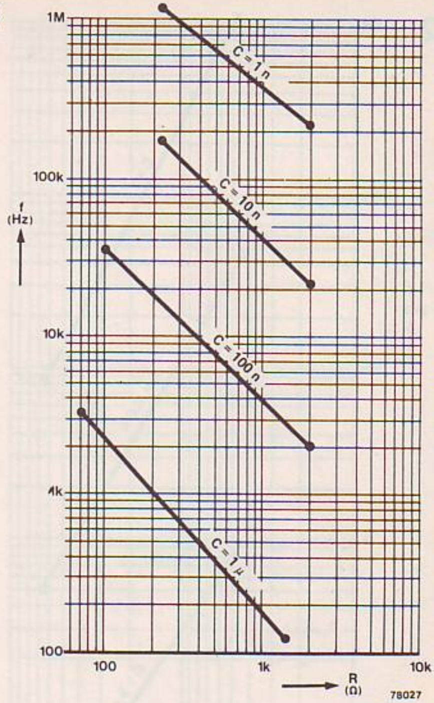

replacing R with a 2.5 k potentiometer in series with a fixed resistor of the minimum permitted value.

A universal squarewave generator of this type can also be constructed using Low Power Schottky TTL or CMOS ICs; both these possibilities are discussed below.

20 Simple LS TTL squarewave generator

The design of this squarewave generator is identical to that of the circuit described above, with the exception that it employs an IC from the increasingly popular Low Power Schottky (LS) TTL series, rather than a conventional TTL IC. Since the electrical characteristics of LS TTL devices differ from those of standard TTL ICs, the relationship between the oscillator frequency and the values of R and C will also be difficult, whilst an extra resistor is required for the circuit to function satisfactorily.

The circuit will generate a squarewave with a

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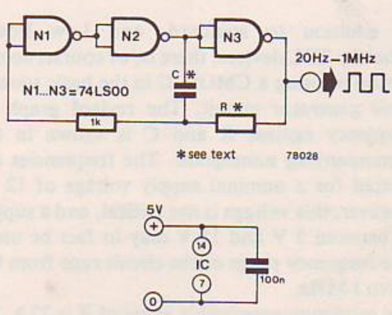

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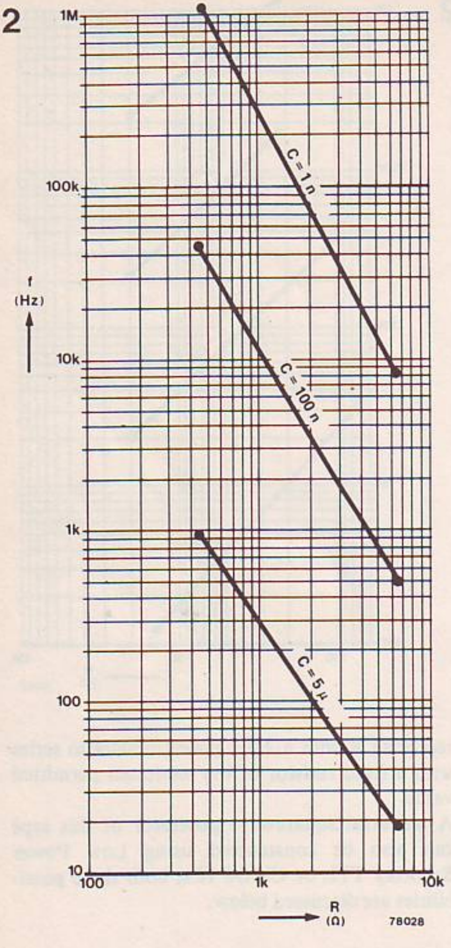

frequency between 20 Hz and 1 MHz. The nomogram once again shows the frequencies obtained for various values of R and C. As was the case in the above circuit, there is a minimum permissible value for R (680 Ω). To obtain a variable squarewave generator, R should be replaced by a 5 or 10 k potentiometer in series with a fixed resistor of 680 Ω .

21 Simple CMOS squarewave generator

In addition to standard- and Low Power Schottky TTL devices, there is, of course, no objection to using a CMOS IC in the basic squarewave generator circuit. The revised graph of frequency against R and C is shown in the accompanying nomogram. The frequencies are plotted for a nominal supply voltage of 12 V, however, this voltage is not critical, and a supply of between 5 V and 15 V may in fact be used. The frequency range of the circuit runs from 0.5 Hz to 1 MHz.

The minimum permissible value of R is 22 k. To

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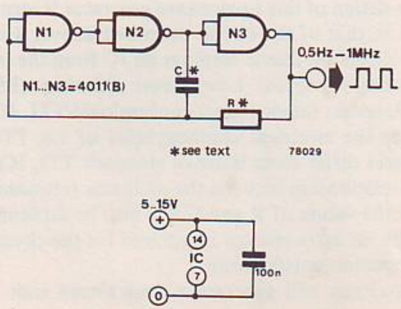

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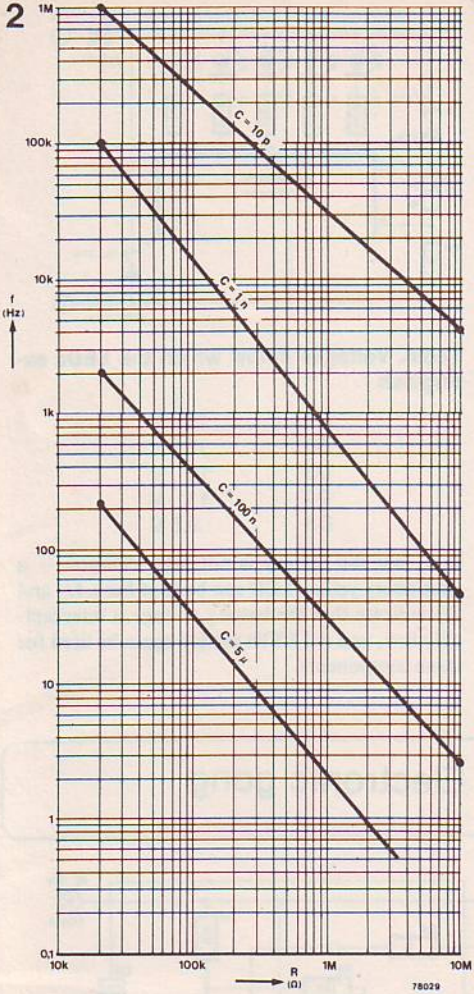

obtain a variable squarewave oscillator, R should be replaced by a fixed value resistor of 22 k in series with a 1 M potentiometer. Both the buffered and unbuffered versions of the 4011 may be used.

22 Automotive voltmeter

Although vital for satisfactory operation of the vehicle, the car battery is often taken for granted and rarely receives adequate maintenance. As a battery ages, its ability to store charge for long periods gradually decreases. The inevitable result is that one morning (usually in the depths of winter) the car fails to start.

The solid-state voltmeter described in this article allows continuous monitoring of the battery voltage so that incipient failure can be spotted at an early stage. The circuit will also indicate any fault in the car voltage regulator which may lead to overcharging and damage to the battery.

Battery voltage can, of course, be measured using a conventional moving-coil voltmeter. However, as only the voltage range from about 9 to 15 V is of interest, only the top third of the scale of a 15 V meter would be used, unless a 'suppressed zero' facility was added. Moving coil meters are also fairly delicate mechanically.

A better solution is to use a solidstate voltmeter which will indicate the voltage on a column of LEDs. Various ICs are available which perform this function. However, the 12 or 16 LED display offered by ICs such as the Siemens UAA 180 and UAA 170 is not required in this application, so an IC was chosen which will drive only five LEDs, the Texas SN 16889P. This IC provides a thermometer-type indication.

The complete circuit of the voltmeter uses only this IC and a handful of other components, since the IC will drive the LEDs directly. Diodes D1 and D2 provide protection against reverse polarity and transients on the supply line, whilst D8 offsets the zero of the meter so that it only begins to read above about 9.5 V. The circuit is calibrated using P1 so that the LEDs extinguish at the voltages shown in the accompanying table. LED D7 will be extinguished below about 15 V. If this LED is lit when the circuit is fitted in the car then the charging voltage is too high and the car voltage regulator is at fault. A red LED should be used for D7. D6 indicates that the battery is fully charged, and a green LED should be used for this component.

D5 indicates that the battery voltage is fairly

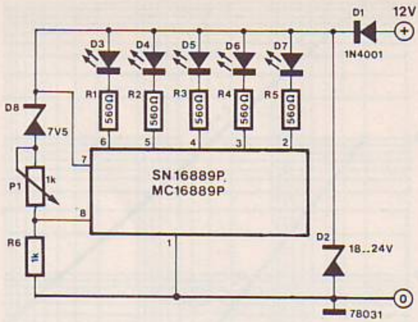

Table. Voltages below which the LEDs extinguish

D7	15 V
D6	13.5 V
D5	12 V
D4	11 V
D3	9.5 V

o.k., but the battery is not fully charged – a cautionary yellow LED can be used here. D4 and D3 indicate that the battery voltage is unacceptably low, and red LEDs should again be used for these components.

23 Electronic gong

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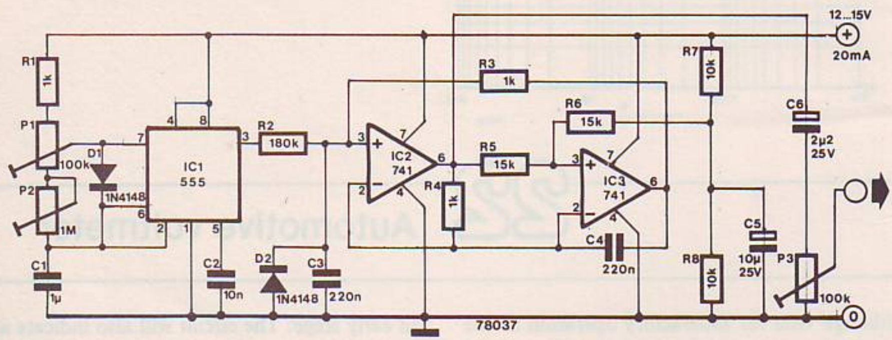

This circuit will simulate the sound of a bell or gong and may be used as a replacement for conventional bells in such applications as doorchimes, clocks etc.

The circuit consists of a resonant filter built around IC2 and IC3 which will ring at its resonant frequency when a short pulse is fed to the input. In this circuit the trigger pulses are provided by a 555 timer connected as an astable multivibrator, but other trigger sources may be used depending on the application.

The character of the sound is influenced by two factors; the Q of the filter, which may be varied by changing the value of R2, and the duration of the trigger pulse, which may be adjusted using P1. The repetition rate of the trigger pulses, i.e.

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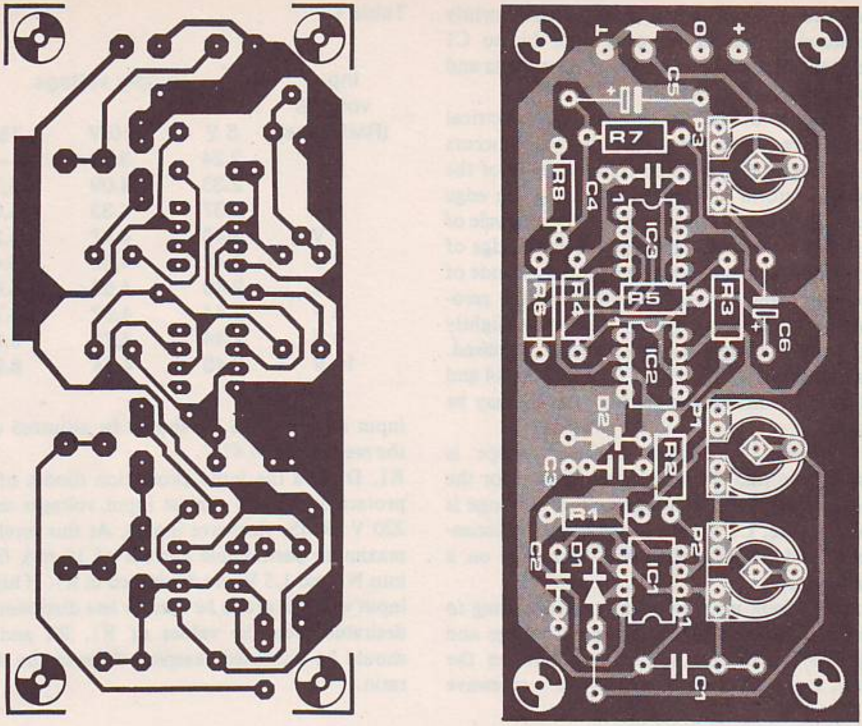
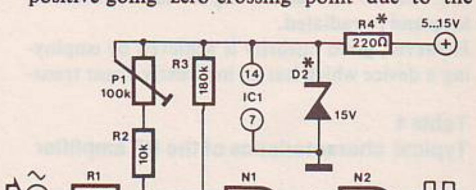


the rate at which the gong is 'struck', may be varied using P2. In order to drive a loudspeaker the output of the circuit must be fed through an audio amplifier. The output level may be varied from zero to about 5 V by means of P3.

24 Zero crossing detector

This circuit will detect precisely the negative-going zero-crossing point of an AC waveform, but requires only a single supply voltage, unlike zero crossing detectors using op-amps. N1 and N2 are Schmitt triggers connected to form a monostable multivibrator with a period of about 15 ms. P1 is adjusted so that when the input voltage falls to zero the voltage at the input of N1 is equal to the low-going threshold of the Schmitt trigger. The output of N1 thus goes high and the output of N2 goes low. C1 holds the second input of N1 below its positive-going threshold for about 15 ms, during which time the output of the circuit will remain low, even if noise pulses on the input waveform should take the first input of N1 high.

When the input signal goes positive the first input of N1 is taken above its positive-going threshold. Note that this occurs after the positive-going zero-crossing point due to the



hysteresis of the Schmitt trigger. Subsequently the second input of N1 goes high due to C1 charging through R3. The circuit then resets and the output of N2 goes high.
The output of N2 is thus an asymmetrical squarewave whose negative-going edge occurs on the negative-going zero-crossing point of the input waveform and whose positive-going edge occurs sometime during the positive half-cycle of the input waveform. The negative-going edge of the waveform is independent of the amplitude of the input signal and occurs always at the zero-crossing point. However, it does vary slightly with supply voltage, so this should be stabilised. If a higher supply than 15 V is used then R4 and D2 must be included, otherwise the IC may be damaged.
To calibrate the circuit an oscilloscope is desirable so that P1 may be set exactly for the zero-crossing point. Alternatively, if a 'scope is not available, C1 should be temporarily disconnected and the output of N2 monitored on a multimeter.
In table 1 look up the voltage corresponding to the RMS input voltage and supply voltage and adjust P1 until this voltage registers on the meter, e.g. with a 10 V supply and a sinewave

Table 1

Input voltage (RMS sine)	Supply voltage 5 V	10 V	15 V
2 V	2.24	3.49	—
3 V	2.33	4.09	5.18
4 V	2.37	4.33	5.91
5 V	2.40	4.47	6.26
6 V	2.42	4.56	6.48
7 V	2.43	4.63	6.64
8 V	2.44	4.67	6.75
9 V	2.44	4.71	6.83
10 V	2.45	4.74	6.90

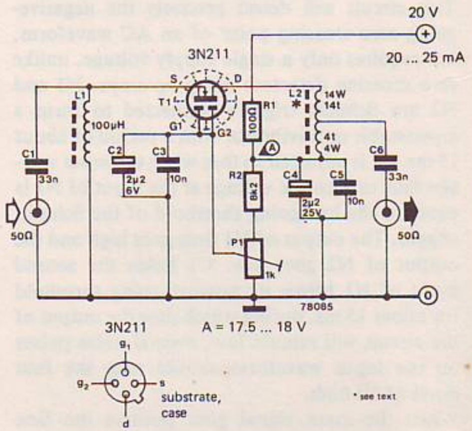
input of 5 V RMS P1 should be adjusted until the meter reads 4.47 V.
R1, D1 and the input protection diodes of N1 protect the circuit against input voltages up to 220 V (RMS, sinewave input). At this level the maximum permissible current of 10 mA flows into N1 and 1.5 W are dissipated in R1. If higher input voltages are to be used or less dissipation is desirable then the values of R1, R2 and P1 should be increased, keeping them in the same ratio.

25 Wideband RF amplifier

This design for an RF amplifier has a large bandwidth and dynamic range, which makes it eminently suitable for use in the front end of a shortwave receiver. The design operates without negative feedback since, if an amplifier with feedback overloads, distortion products can be fed back to the (aerial) input via the feedback loop and re-radiated.
However, good linearity is achieved by employing a device which has an inherently linear transfer characteristic, in this case a dual-gate MOSFET with both gates linked. With the 3N211 used in this circuit the transconductance of the device is constant at about 14 mA/V pro-

Table 1
Typical characteristics of the RF amplifier

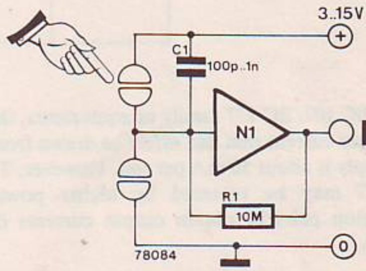
gain: approximately 10 dB
3 dB bandwidth: 4 MHz to 55 MHz
noise figure: less than 5 dB
two-tone test:
  output power for third order
  IM distortion at − 40 dB with respect to
  one tone: + 22 dBm/tone



vided the drain current is greater than approximately 12.5 mA.
The MOSFET is used in a commongate configuration, with P1 used to set the drain current at around 20 mA. One home-made inductor is employed in the circuit, L2, which is wound on a Philips/Mullard type 4312-020-31521, two-hole ferrite bead, sometimes referred to as a 'pig's nose ferrite bead'. 14 turns of 31 SWG (0.3 mm) enamelled copper wire are wound through one hole of the bead and four turns are wound through the other hole, one end of each winding being joined to form the tap which connects to C6.
P1 should be adjusted so that the voltage at the test point shown in figure 1 is between 17.5 V and 18 V.

26 Super-simple touch switch

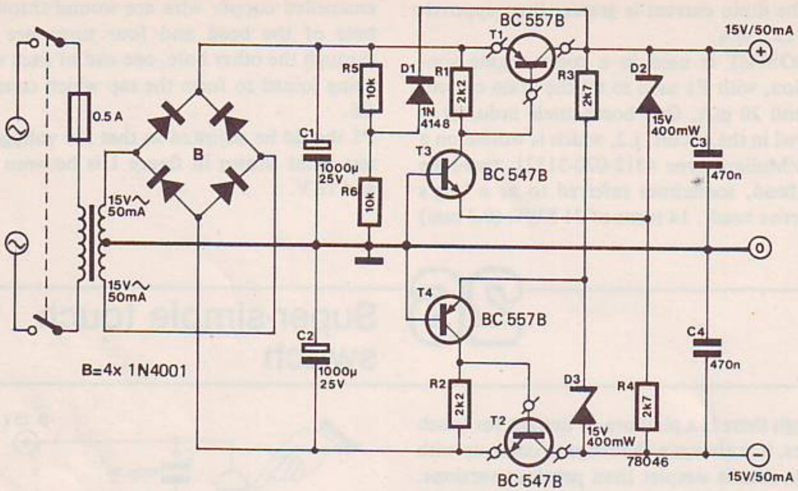
Although there is a plethora of designs for touch switches, it is always a challenge to come up with a design that is simpler than previous versions. While most latching touch switches use a pair of NAND gates connected as a flip-flop, this circuit uses only one non-inverting CMOS buffer, one capacitor and a resistor. When the input of N1 is taken low by bridging the lower pair of touch contacts with a finger, the output of N1 goes low. When the contacts are released the input of N1 is held low by the output via R1, so the output remains low indefinitely. When the upper pair of contacts is bridged the input of N1 is taken high, so the output goes high. When the contacts are released the input is still held high via R1, so the output remains high.



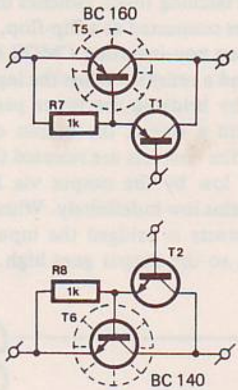
27 Symmetrical ± 15 V/50 mA supply

Although IC voltage regulators have now largely displaced discrete component designs, this circuit offers a considerable cost advantage over an IC regulator.

Operation of the circuit is extremely simple. The centre-tapped transformer, bridge rectifier and reservoir capacitors C1 and C2 provide an unregulated supply of about ±20 V. The positive and negative regulators function in an identical manner except for polarity, so only the positive regulator will be described in detail.
The positive supply current flows through a series regulator transistor T1. 15 V is dropped across zener diode D5, the upper end being at about +15 V and the lower end at 0 V. Should the output voltage of the regulator tend to fall then the lower end of D5 will fall below 0 V and transistor T3 will draw more current. This will supply T1 with more base current, turning it on harder so that the output voltage of the regulator will rise. If the output voltage of the regulator is too high then the reverse will happen. The potential at the lower end of D5 will rise and T3 will draw less current. T1 in turn will tend to turn off and the supply voltage will fall. The negative supply functions in a similar manner. Since D5 and D6 receive their bias from the output of the supply, R5, R6 and D7 must be included to make the circuit self-starting. An initial bias of about 10 V from the unregulated supply is provided by these components. Once the output voltage of the supply has risen to its normal value D7 is reverse-biased, which prevents ripple from the unregulated supply appearing on the output.
Using inexpensive small-signal transistors such



as the BC 107/BC 177 family or equivalents, the maximum current that can safely be drawn from the supply is about 50 mA per rail. However, T1 and T2 may be replaced by higher power Darlington pairs to obtain output currents of 500 mA.



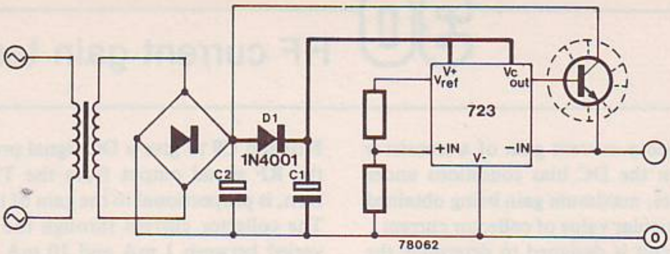
28 Improved 723 supply

The 723 is a very widely used IC regulator. Hence the following circuit, which is intended to reduce power dissipation when the 723 is used with an external transistor, should prove very popular. According to the manufacturer's specification the supply voltage to the 723 should always be at least 8.5 V to ensure satisfactory operation of the internal 7.5 V reference and of the IC's internal differential amplifier.

Using the 723 in a low-voltage high-current supply, with an external series transistor operating from the same supply rail as the 723, invariably results in excessive dissipation in the series transistor. For example, in a 5 V 2 A supply for TTL about 3.5 V would be dropped across the series transistor and 7 W would be dissipated in it at full load current. Furthermore, the reservoir capacitor must be larger than necessary to prevent the supply to the 723 falling below 8.5 V in the ripple troughs.

In fact the supply voltage to the series transistor need be no more than 0.5 V above the regulated output voltage, to allow for its saturation voltage.

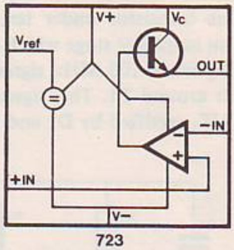
The solution is to use a separate 8.5 V supply for the 723 and a lower voltage supply for the external transistor. Rather than using separate transformer windings for the two supplies, the supply



to the 723 is simply tapped off using a peak rectifier D1/C1. Since the 723 takes only a small current C1 will charge up to virtually the peak voltage from the bridge rectifier, 1.414 times the RMS voltage of the transformer minus the voltage drop of the bridge. The transformer voltage thus needs to be at least 7 V to give an 8.5 V supply to the 723.

However, by suitable choice of reservoir capacitor C2 the ripple on the main unregulated supply can be made such that the voltage falls to about 0.5 V above the regulated output voltage in the ripple troughs. The average voltage fed to the series transistor will thus be less than 8.5 V and the dissipation will be greatly reduced.

The value of C1 is determined by the maximum base current that the 723 must supply to the



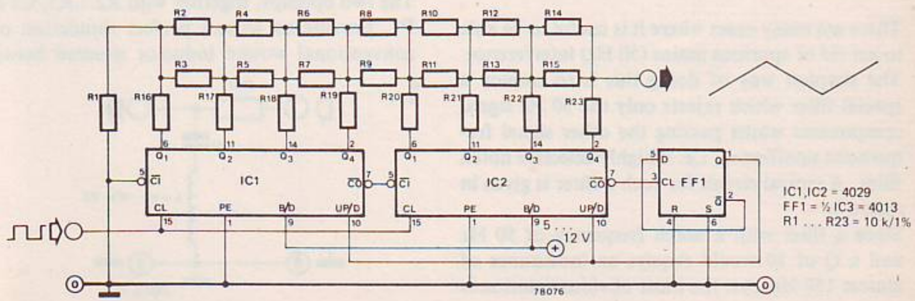
series output transistor. As a rule of thumb allow about 10 μF per mA. The base current can be found by dividing the maximum output current by the gain of the transistor. A suitable value for the main reservoir capacitor C2 is between 1500 and 2200 μF per amp of output current.

29 Squarewave-staircase converter

This circuit can be used to generate an up-down staircase waveform with a total of 512 steps per cycle. IC1 and IC2 are two four-bit up-down counters connected as an 8-bit counter, with an R-2R D-A ladder network connected to the outputs to convert the binary output codes to a staircase waveform.

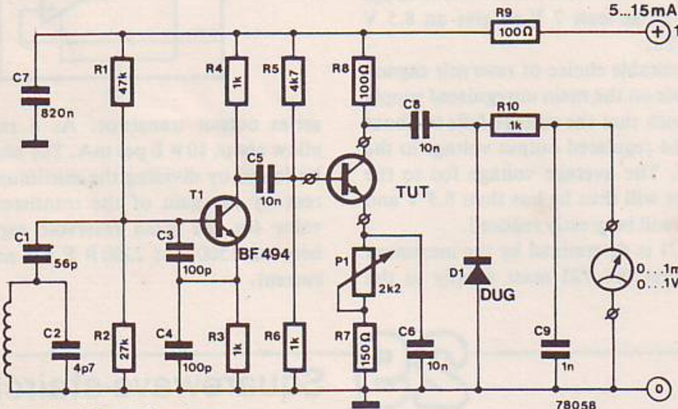
When a squarewave is fed to the clock input the circuit will count up until the counter reaches 255, when the carry output will go low and clock FF1. The circuit will then count down until zero is reached, when the carry output will again clock FF1 and so on.

To ensure that the staircase steps are of equal height 1% tolerance resistors should be used for R1 to R23.



30 HF current gain tester

The high-frequency current gain of a transistor is dependent on the DC bias conditions under which it operates, maximum gain being obtained at only one particular value of collector current. This simple circuit is designed to determine the optimum collector current for any NPN RF transistor. The transistor under test (TUT) is inserted into an amplifier stage which is fed with a constant amplitude 100 MHz signal from an oscillator built around T1. This signal is amplified by the TUT, rectified by D1 and filtered by R10 and C9 to give a DC signal proportional to the RF signal output from the TUT. This, in turn, is proportional to the gain of the TUT.
The collector current through the TUT can be varied between 1 mA and 10 mA by means of P1, which should be fitted with a scale marked out linearly between these values. It is then a simple matter to adjust P1 until the maximum output voltage is obtained on the meter, whereupon the optimum collector current can be read off from the scale of P1.



L1 = 5 Wdg. 0,8 mm Cu ϕ 6 mm
L1 = 5 turns 0.8 mm (21 SWG) Cu ϕ 6 mm

31 Hum filter

using electronically simulated inductor

There are many cases where it is useful to be able to get rid of spurious mains (50 Hz) interference. The simplest way of doing this is to employ a special filter which rejects only the 50 Hz signal components whilst passing the other signal frequencies unaffected, i.e. a highly selective notch filter. A typical circuit for such a filter is given in figure 1.
Since a filter with a notch frequency of 50 Hz and a Q of 10 would require an inductance of almost 150 Henrys, the most obvious solution is to synthesise the required inductance electronically (see figure 2).
The two opamps, together with R2...R5, C2 and P1, provide an almost perfect simulation of a conventional wound inductor situated between

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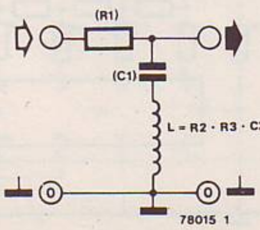

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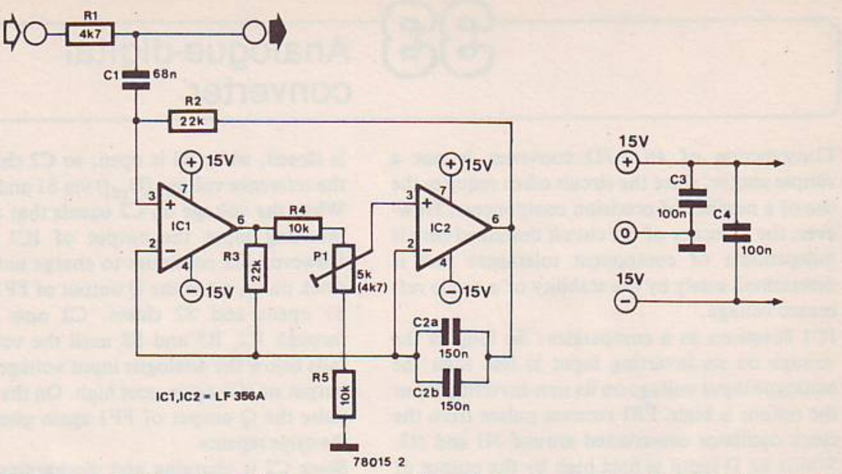


pin 3 of IC1 and earth. The value of inductance thereby obtained is equal to the product of the values of R2, R3 and C2 (i.e. L = R2 x R3 x C2). For tuning purposes this value can be varied slightly by means of P1. If the circuit is correctly adjusted, the attenuation of 50 Hz signals is 45 to 50 dB. The circuit can be used as it stands as a hum rejection filter in harmonic distortion meters or as a hum filter for TV sound signals.

32 Voltage mirror

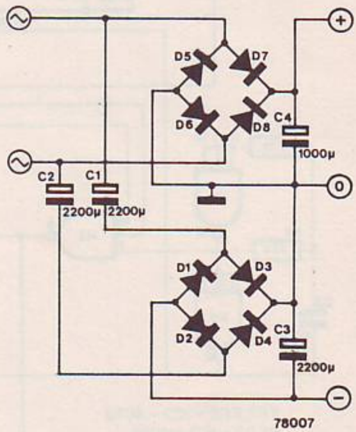
There are a number of different ways of using a transformer with only one secondary winding to obtain both a positive and a negative supply voltage. This design is a contribution towards such a the discussion.

The circuit uses a second bridge rectifier (D1...D4) which, via C1 and C2, is capacitively-coupled to the transformer. Since the resultant voltage is DC-isolated from the transformer, to which the other rectifier (D5...D8) is connected, the positive terminal of C3 can be linked directly to the 0 V rail to give a symmetrical ± supply.

Since (because of C1 and C2) C3 is charged from a higher impedance than C4, this capacitor should have a higher value than C4, otherwise the internal impedance and ripple voltage of the negative supply will differ significantly from it's positive counterpart.

The working voltages of the capacitors should at least equal the peak value of the transformer voltage. With the values given in the diagram the circuit will supply approx. 0.1 A for a transformer voltage of 15 V and a ripple voltage of 1 V.

Naturally enough all the capacitance values can



be increased by the same factor in order to reduce the ripple voltage.

As far as the bridge rectifiers are concerned, these should be adequately rated to withstand the peak transformer voltage and the maximum load current.

H. Springer

33 Analogue-digital converter

Construction of an A/D converter is not a simple matter, since the circuit often requires the use of a number of precision components. However, the accuracy of the circuit described here is independent of component tolerances and is determined solely by the stability of a single reference voltage.

IC1 functions as a comparator. So long as the voltage on its inverting input is less than the analogue input voltage on its non-inverting input the output is high. FF1 receives pulses from the clock oscillator constructed around N1 and N2. Whilst its D input is held high by the output of IC1 its Q output remains high. CMOS switch S1 is closed, while S2 is open, so C2 charges from the reference voltage (U_{ref}) via S1 and R2.

When the voltage on C2 equals that at the non-inverting input the output of IC1 goes low. However, C2 continues to charge until the next clock pulse, when the Q output of FF1 goes low, S1 opens and S2 closes. C2 now discharges through R2, R5 and S2 until the voltage on it falls below the analogue input voltage, when the output of IC1 again goes high. On the next clock pulse the Q output of FF1 again goes high and the cycle repeats.

Since C2 is charging and discharging exponentially it follows that the higher the analogue

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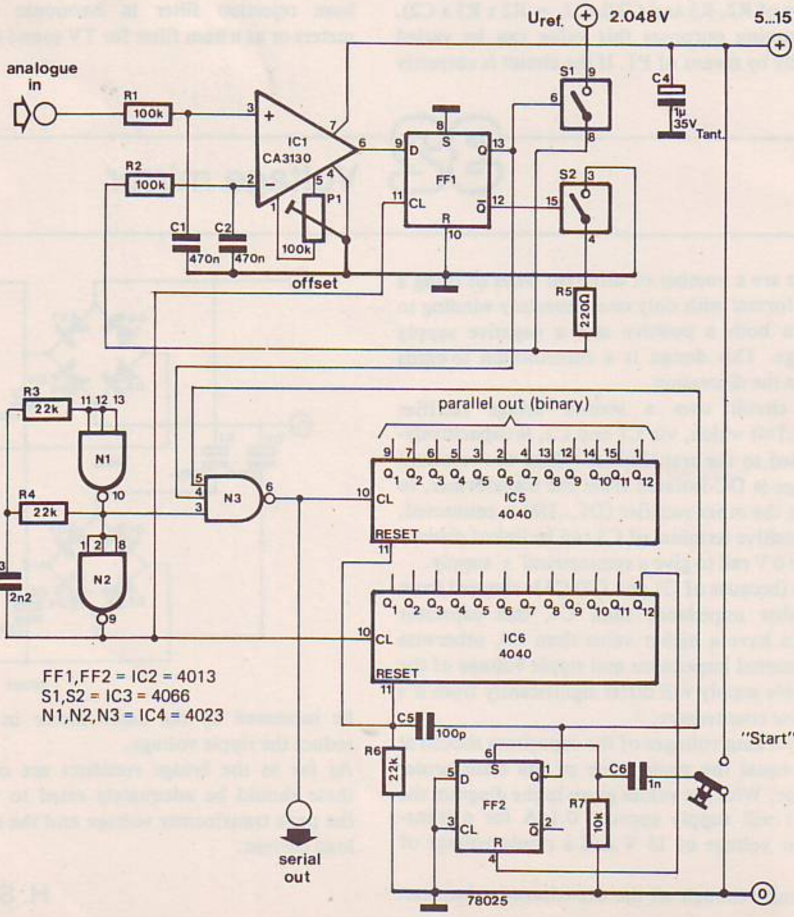

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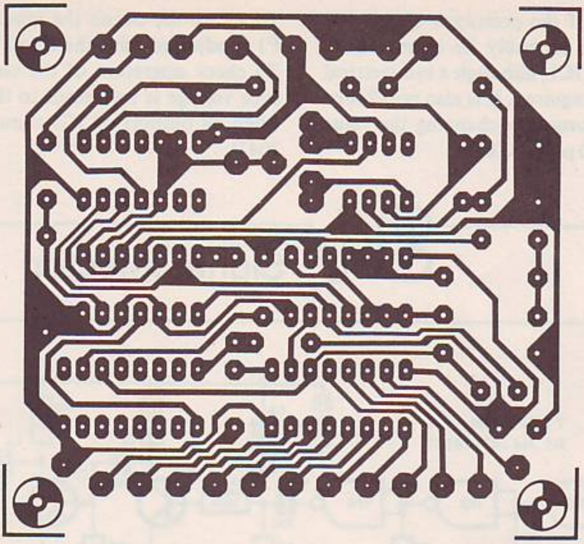
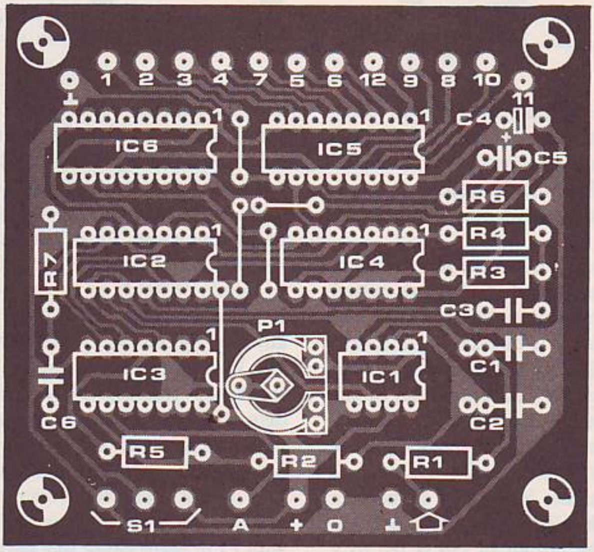




input voltage the longer will be the charge periods of C2 and the smaller will be the discharge periods. The result is that the output of IC1 is a squarewave whose duty-cycle is proportional to the analogue input voltage. Note that this only applies once the circuit has reached equilibrium. It does not apply during the initial phase when C2 is charging from zero.

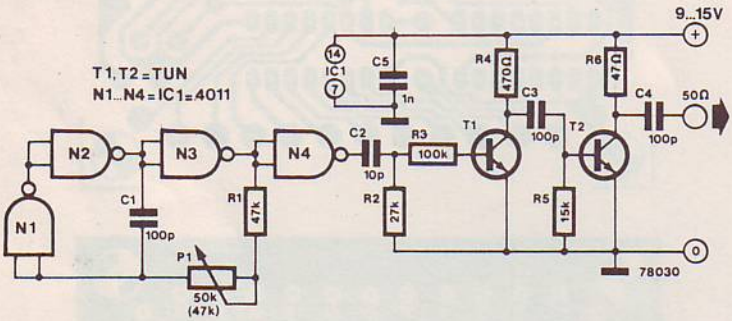
When the 'start conversion' switch is closed flip-flop FF2 is set. This enables counters IC5 and IC6. Both count clock pulses, but while IC6 counts every clock pulse IC5 counts clock pulses only whilst the Q output of FF1 is high. When the Q_{12} output of IC6 goes high FF2 is reset and the conversion ceases. The count which IC5 has reached is thus proportional to the duty-cycle of the Q output of FF1, which is proportional to the analogue input level.

If the reference voltage is exactly 2.048 V then the count of IC5 will be 1000 for an input of 1

volt. The linearity of the prototype circuit was 1%, but this could probably be improved by using an LF 357 for IC1, although a symmetrical supply will then be required. It is also possible to vary the clock frequency by changing the value of C3 (minimum 390 p for 50 kHz).

To set up the circuit the input is grounded and P1 is adjusted until the count from IC5 is zero. To check operation of the converter the reference voltage is connected to the analogue input when all outputs of IC5 should be high (count 2047).

34 Signal injector

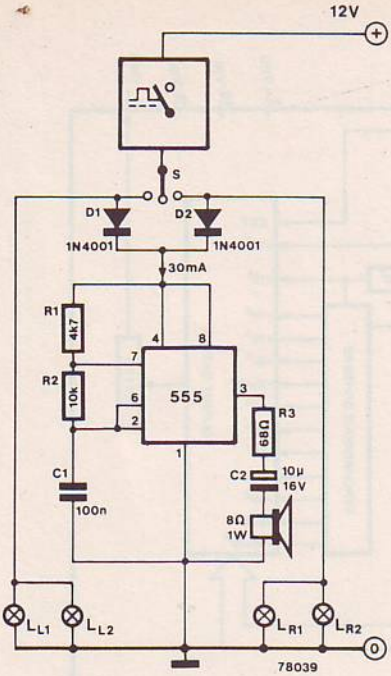


This simple signal injector should find many uses in trouble shooting and alignment applications. It produces an output with a fundamental frequency of 100 kHz and harmonics extending up to 200 MHz and has an output impedance of 50 ohms.

N1, N2 and N3 form an astable multivibrator with a virtually symmetrical squarewave output and a frequency of approximately 100 kHz. The output of the oscillator is buffered by a fourth NAND gate N4. Since the squarewave is symmetrical it contains only odd harmonics of the fundamental frequency, the higher harmonics being fairly weak due to the relatively slow rise time of the CMOS devices employed. As it is necessary for the higher harmonics to be at a reasonable level if the circuit is to prove useful at high frequencies, the output of N4 is fed to a differentiating network R2/C2. This attenuates the fundamental relative to the harmonics, producing a needle-pulse waveform which is then amplified by T1 and T2. This is rich in harmonics and, due to the extremely small duty-cycle of the waveform, the power consumed by the output stage, T2, is fairly small. The output frequency of the signal injector can be adjusted by means of P1. If an accurate output frequency is required then the signal injector can be adjusted by beating its second harmonic with the 200 kHz Droitwich broadcast transmitter. The frequency stability of the circuit is largely determined by the construction. To minimise hand capacitance effects the unit should be housed in a metal box for screening, with the only output connection being the signal probe. If desired, a 1 k preset may be included in series with P1 to allow easier fine tuning.

35 Flasher bleeper

Although extremely useful, the selfcancelling devices fitted to car direction indicators are not infallible. For example, they will not operate when only a small movement of the steering wheel is made, as when pulling out to overtake. An audible warning device to indicate that the



flashers have not cancelled is preferable to the visual indication normally fitted, as it is more noticeable and does not require the driver to take his eyes off the road.
The circuit consists simply of a 555 timer connected as a 1 kHz astable multivibrator. The output of the 555 is more than sufficient to drive a small loudspeaker. When the trafficator switch (S) is set to either the left or right positions, power is supplied to the multivibrator via the flasher unit and D1 or D2. The circuit thus 'beeps' with the same rhythm as the flashing of the indicators. If desired, the volume can be reduced by increasing the value of R3. The 'beep' frequency is determined by C1. For operation in positive earth cars D1 and D2 should be reversed and the multivibrator circuit turned upside-down, i.e. the C1/pin 1/loudspeaker junction is connected to the commoned anodes of the diodes and the R1/pin 4/pin 8 junction is connected to supply common.

36 IC counter timebase

A Mostek IC, the MK 5009, is a complete timebase for frequency counters and other applications. The internal block diagram of the IC is shown in figure 1. It incorporates a clock circuit (which may be used either with an external reference frequency, with an external RC circuit or with an external crystal) and a programmable divider. By applying an appropriate binary code to the programming inputs the division ratio may be varied in decade steps from 10^0 to 10^8. Other division ratios are also available, the most interesting being divide-by- 2×10^4, which gives a 50 Hz output with a 1 MHz clock frequency or a 60 Hz output with a 1.2 MHz clock frequency.
A practical circuit using the MK 5009 is shown in figure 2, whilst table 1 shows the division ratios that may be obtained for the different settings of S1 to S4. A 1 MHz crystal is used in a parallel resonant circuit and this crystal should be a 30 p parallel resonant type.
The divided down output is available at pin 1 of the IC. This output will drive CMOS circuits or one TTL unit load directly. However, since the IC is fairly expensive it is recommended that a permanent buffer stage be connected to the output. This may take the form of a TTL or CMOS

S1	S2	S3	S4	division ratio
0	0	0	0	10^0
0	0	0	1	10^1
0	0	1	0	10^2
0	0	1	1	10^3
0	1	0	0	10^4
0	1	0	1	10^5
0	1	1	0	10^6
0	1	1	1	10^7
1	0	0	0	10^8
1	0	0	1	6×10^7
1	0	1	0	36×10^8
1	0	1	1	6×10^8
1	1	1	0	2×10^4

0 = switch closed
1 = switch open

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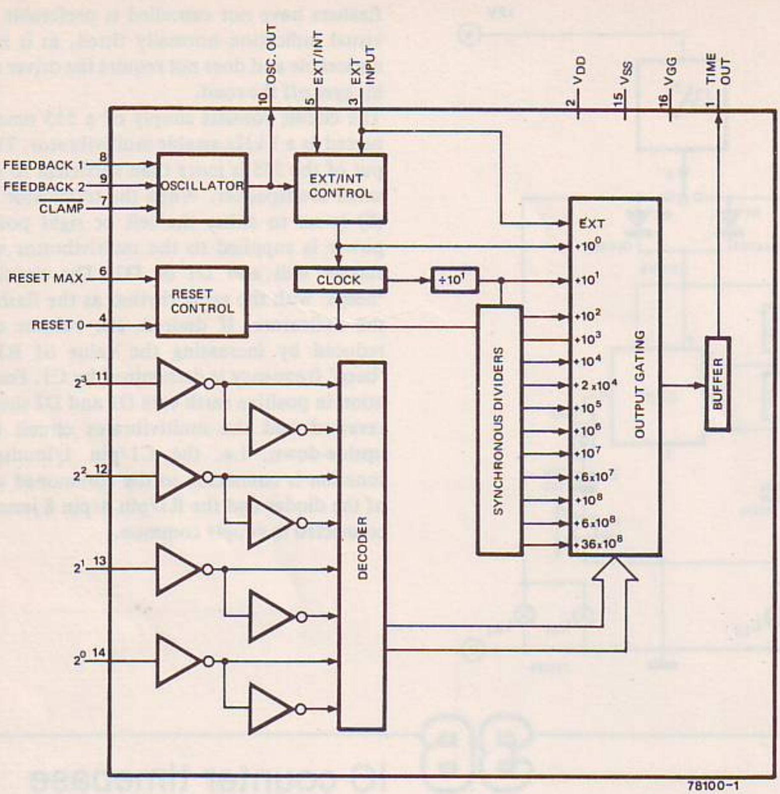
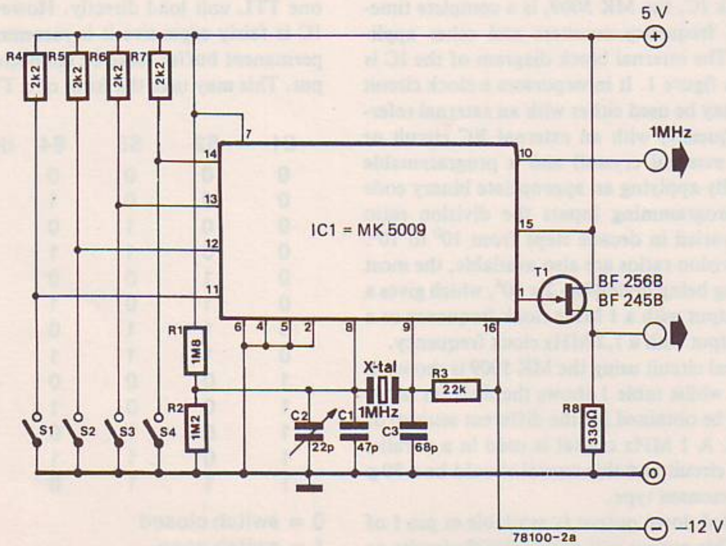


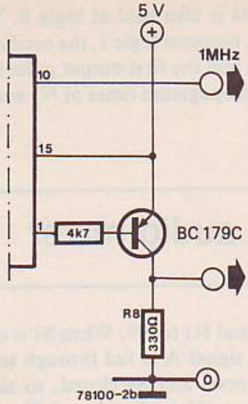
OSC. OUT
EXT/INT
EXT INPUT
VDD
VSS
VGG
TIME OUT
FEEDBACK 1
FEEDBACK 2
CLAMP
OSCILLATOR
EXT/INT CONTROL
RESET MAX
RESET CONTROL
RESET 0
CLOCK
÷10¹
EXT
÷10⁰
÷10¹
÷10²
÷10³
÷10⁴
÷2 x10⁴
÷10⁵
÷10⁶
÷10⁷
÷6x10⁷
÷10⁸
÷6x10⁸
÷36x10⁸
SYNCHRONOUS DIVIDERS
OUTPUT GATING
BUFFER
DECODER
2³
2²
2¹
2⁰
78100-1

2a

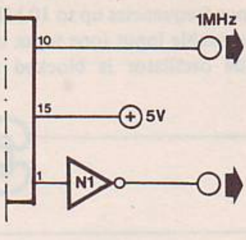


5 V
R4
R5
R6
R7
2k2
1MHz
IC1 = MK 5009
T1
BF 256B
BF 245B
R1
1M8
R2
1M2
X-tal
1MHz
R3
22k
R8
330Ω
C2
22p
C1
47p
C3
68p
S1
S2
S3
S4
0
−12 V
78100-2a

2b



2c



gate or buffer, a FET or a bipolar transistor. The 1 MHz clock frequency is available at pin 10 of the IC and must similarly be buffered if it is to be used.

Trimming of the oscillator frequency for maximum accuracy can be carried out using C2. With the division ratio set to 10, C2 can be adjusted for zero beat between the output and an accurate frequency such as the 200 kHz Droitwich transmitter.

37 Stable-Start-Stop-Squarewave

In digital circuits where parallel information must be converted into serial data, a start-stop oscillator is often used. One system is to use the oscillator to clock a counter, the output of which is compared with the parallel data. Initially the counter is reset; the external oscillator is then started, clocking the counter; when the correct count is reached, the oscillator is stopped. The result is a (clock) pulse train, the length of which corresponds to the binary number given by the parallel data. It is not sufficient for these applications to gate the output of a free-running oscillator, since the 'enable' signal is not normally synchronised to the oscillator. The circuit de-

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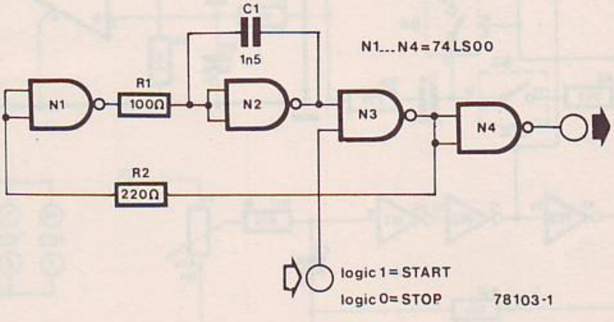

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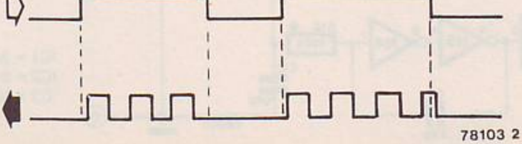
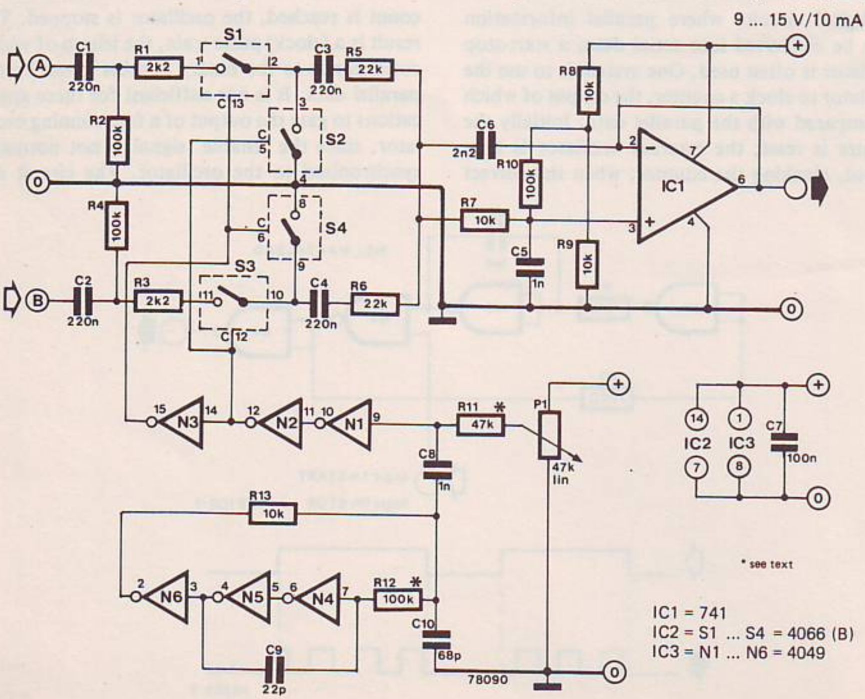


scribed here is actually turned on and off by the enable signal, and it has proved reliable and stable for output frequencies up to 10 MHz.
As long as the enable input (one input of N3) is at logic 0, the oscillator is blocked and the output of N4 is also held at logic 0. When the enable input becomes logic 1, the oscillator starts immediately and the first output pulse is delayed only by the propagation times of N3 and N4.

38 Digital audio mixer

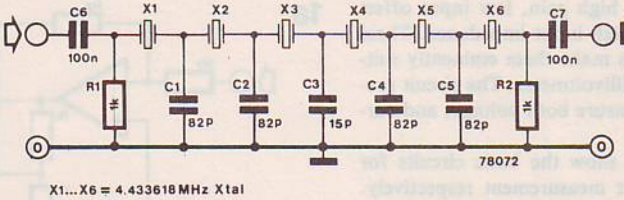
A novel approach is employed in this circuit, which allows mixing of two audio signals and cross-fading between them. Rather than using conventional potentiometers as analogue attenuators together with a summing amplifier, the circuit functions by sampling the two signals alternately at a high frequency.
The input signals are fed to a pair of electronic switches each comprising two elements of a 4066 CMOS analogue switch IC. The use of a switch in shunt with the signal path as well as in series allows a high load impedance to be used (for low distortion) whilst at the same time maintaining good signal isolation when the switch is 'off'. The two switches are opened and closed alternately by a 100 kHz, two-phase clock constructed around N1 to N6. When S1 is closed, S2 is open and signal A is fed through to IC1. S3 however, is open and S4 closed, so signal B is blocked. When S3 is closed and S1 open then signal B is, of course, passed while A is blocked. P1 allows the duty-cycle of the clock pulses to be adjusted, i.e. the proportion of the total time for which each signal is passed. This in turn varies the amplitude of each signal. With P1 in its mid-position both signals have approximately the same amplitude whilst at the two extremes one signal is completely blocked whilst the other is passed continuously.
A lowpass filter built around IC1 removes any clock frequency components from the output. Although these are inaudible they could, if not



filtered out, damage power amplifiers and loudspeaker tweeters or beat with the bias oscillator in a tape recorder to cause high-pitched bleeping tones.
The supply voltage, which should be stabilised and ripple-free, may lie between 9 V and 15 V. Above 15 V the CMOS ICs may be damaged and below 9 V the 741 will not function satisfactorily. The maximum input signal that the circuit will accept without distortion is about 1 V RMS.

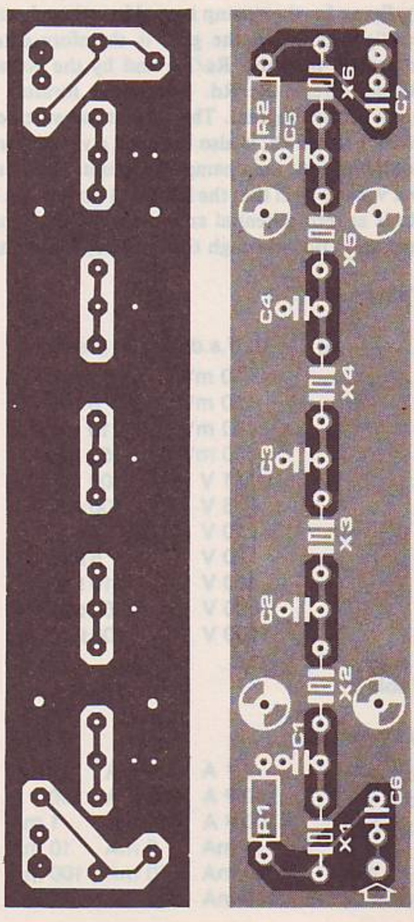
39 Cheap crystal filter

1



In view of the dramatic drop in the price of crystals used in colour TV sets, they now represent an economical way of building an SSB-filter. The circuit shown in the accompanying diagram is for a filter with a −6 dB bandwidth of roughly 2.2 kHz.
The layout for the p.c.b. indicates how such a circuit can be constructed. This type of arrangement has the advantage that the input and out-

2



Parts list.

Resistors:
R1, R2 = 1 k

Capacitors:
C1, C2, C4, C5 = 82 p
C3 = 15 p
C6, C7 = 100 n ceramic

Miscellaneous:
X1, X2, X3, X4, X5, X6 = 4.433,618 kHz

Table.

f_0	4432,03 kHz		
$f_{-6\,dB}$ (r)	4433,06 kHz	B − 6 dB	2,26 kHz
$f_{-6\,dB}$ (l)	4430,70 kHz		
$f_{-60\,dB}$ (r)	4435,30 kHz	B − 60 dB	7,90 kHz
$f_{-60\,dB}$ (l)	4427,40 kHz		
slope factor (r)	1:3,17		
slope factor (l)	1:3,48		
ripple	2 dB		

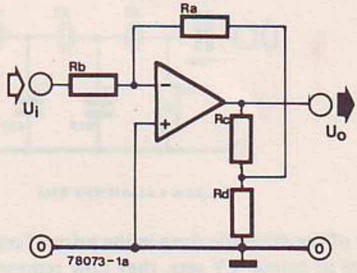
put are as far as possible apart from one another, so that rejection outside the passband is at a maximum. By terminating the input and output with a 1 k resistor in parallel with an 18 p trimmer capacitor, passband ripple can be tuned down to 2 dB. The most important specs are given in the accompanying table, to which should be added that the out-of-band attenuation is 90 dB.

40 FET millivoltmeter

FET opamps have high gain, low input offset and an extremely high input impedance. These three characteristics make them eminently suitable for use in a millivoltmeter. The circuit presented here can measure both voltages and currents.

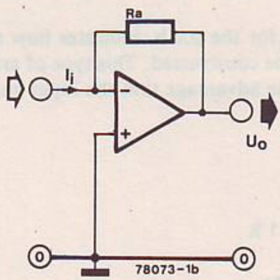
Figures 1a and 1b show the basic circuits for voltage and current measurement respectively. In figure 1a, the opamp is used in a virtual earth configuration and the gain is therefore determined by the ratio Ra/Rb and by the voltage divider circuit Rc/Rd. The exact formula is given in the diagram. The current measurement circuit, figure 1b, is also basically a virtual earth configuration; the opamp will maintain an output voltage such that the left-hand (input) end of Ra is at zero potential and, since the input current must flow through this resistor, the voltage drop across Ra equals I x Ra. Therefore, the output voltage must − I x Ra.

1a



$$U_o = -U_i \frac{R_a}{R_b} \frac{R_c + R_d}{R_d}$$

1b



$$U_o = -I_i R_a$$

The complete circuit (figure 2) combines these two functions. The range switch S3 selects the required feedback resistor (Ra in figure 1) and the voltage divider (Rc and Rd) if the latter is required. The resulting ranges are listed in Table 1. The polarity of the meter can be reversed by means of switch S2.

A symmetrical +/−3 V supply is required, capable of delivering 1 mA. This low voltage and low current consumption means that the FET millivoltmeter can be battery-powered. This is a highly desirable feature, since the meter can then be used for so-called 'floating' measurement. A higher supply voltage is permissible, if it is easier

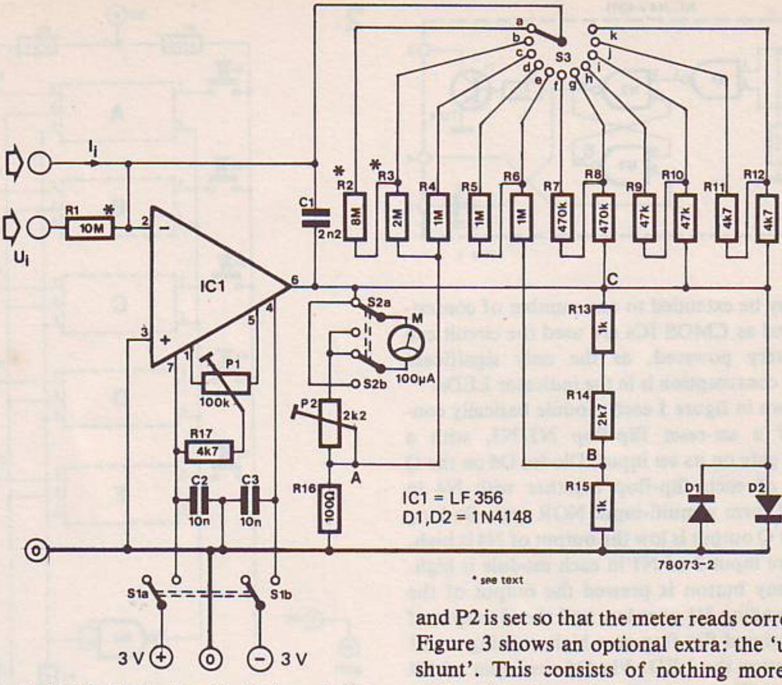
Table 1

S3	U_i (f.s.d.)	I_i (f.s.d.)
a	10 mV	1 nA
b	50 mV	5 nA
c	100 mV	10 nA
d	500 mV	50 nA
e	1 V	100 nA
f	5 V	500 nA
g	10 V	1 µA
h	50 V	5 µA
i	100 V	10 µA
j	500 V	50 µA
k	1000 V	100 µA

Table 2

S3 in position:	a	b	c
I_a (f.s.d.)	1 µA	5 µA	10 µA
I_b (f.s.d.)	10 µA	50 µA	100 µA
I_c (f.s.d.)	100 µA	500 µA	1 mA
I_d (f.s.d.)	1 mA	5 mA	10 mA
I_e (f.s.d.)	10 mA	50 mA	100 mA
I_f (f.s.d.)	100 mA	500 mA	1 A

2



to obtain (4.5 V flat batteries, for instance); the maximum for these opamps is a symmetrical +/−16 V supply.

It is advisable to use 1% resistors, and P1 and P2 should preferably by high-quality preset potentiometers. R1, R2 and R3 may prove difficult to obtain, in which case a series-chain of 1 M resistors must be used.

Preset P1 is for offset compensation. With the meter input shorted, this preset is adjusted until the meter reads zero. P2 is the calibration potentiometer: a known voltage (or current) is applied and P2 is set so that the meter reads correctly.

Figure 3 shows an optional extra: the 'universal shunt'. This consists of nothing more than a chain of resistors that can be connected across the voltage input terminals of the meter. If current is passed through any one of these resistors, a corresponding voltage drop will appear across this resistor. Since there is no voltage drop across any of the other resistors, this voltage will be indicated by the meter. Table 2 lists the resulting current measurement ranges. As before, 1% resistors should be used for the actual measuring chain (R19...R24).

J. Borgman

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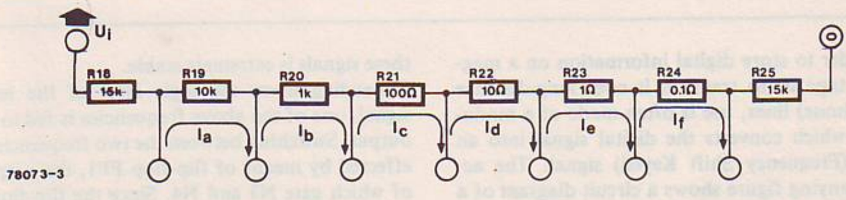
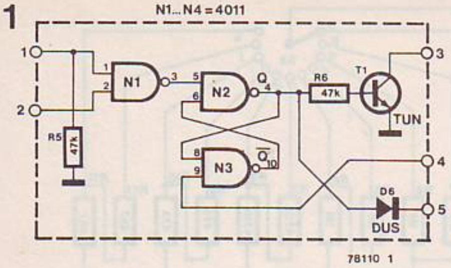
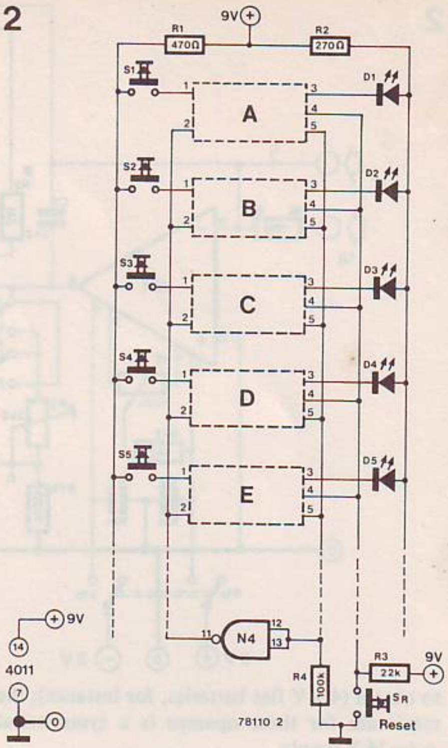


41 Quizmaster

In many quiz games speed of response plays an essential part, the contender who presses a button first getting the first chance of answering a question. The circuit shown here is designed to determine and indicate which contestant is 'quickest on the draw'. The design is modular





and may be extended to any number of contestants, and as CMOS ICs are used the circuit can be battery powered, as the only significant current consumption is in the indicator LEDs.

As shown in figure 1 each module basically consists of a set-reset flip-flop N2/N3, with a NAND gate on its set input. Diodes D6 on the Q output of each flip-flop together with N4 in figure 2 form a multi-input NOR gate. So long as every Q output is low the output of N4 is high, therefore input 2 of N1 in each module is high. When any button is pressed the output of the corresponding N1 goes low and the Q output of the associated flip-flop goes high, turning on T1 and lighting the LED. Via D6 the input of N4 goes high. The output thus goes low, taking the inputs of all N1's low and inhibiting the pushbuttons so that no other flip-flop may be set.

The flip-flop which has been set may be reset ready for the next question by pushbutton S_R. By connecting additional modules as shown in figure 2 the circuit may be extended almost indefinitely. If desired the output of N4 may be used to drive a buzzer via a buffer transistor.

P. Wendt

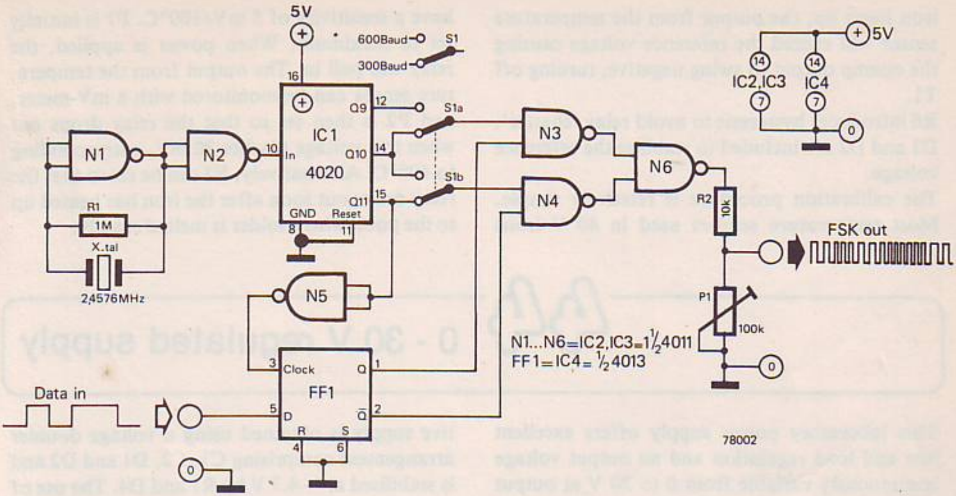
42 CMOS FSK modulator

In order to store digital information on a magnetic tape or to transmit it over long-distance (telephone) lines, use is often made of a modulator which converts the digital signal into an FSK (Frequency Shift Keyed) signal. The accompanying figure shows a circuit diagram of a simple and reliable FSK modulator which has the advantage of requiring no calibration.

A crystal oscillator supplies a reference pulse train which is fed to the input of a counter, IC1. At the Q10 output of this counter is a signal with a frequency of approx. 2,400 Hz, whilst a signal with exactly half that frequency, i.e. approx. 1,200 Hz, is available at the Q11 output. Since a crystal oscillator is used, the frequency of both these signals is extremely stable.

Depending upon the logic level of the input signal, one of the above frequencies is fed to the output. Switching between the two frequencies is effected by means of flip-flop FF1, the outputs of which gate N3 and N4. Since the flip-flop is clocked by the 1,200 Hz signal, the FSK signal will always consist of 'complete' cycles of both 1,200 and 2,400 Hz. This arrangement is necessary to facilitate demodulation of the FSK signal.

With switch S1 in the position shown in the diagram, the modulator will output data at a speed of 300 Baud (= bits per second). By changing over the position of this switch a transmission rate of 600 Baud can be obtained, in which case



the frequencies used then become 2,400 and 4,800 Hz. Since the number of bits *per cycle* therefore remains the same, the reliability of the modulator is not affected.

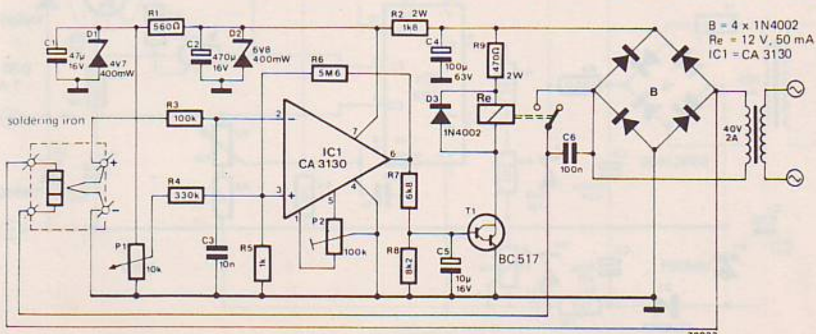
The amplitude of the output signal can be varied by means of P1. If the modulator is used with a cassetterecorder, it may prove necessary to include a lowpass filter between the modulator output and the recorder. A simple RC network with a break frequency of roughly 5 kHz should do the trick.

Although it is in fact available, the crystal (2.4576 MHz) may prove difficult to track down, in which case one can, of course, experiment with other crystal values and other counter outputs.

H.W. Braun

43 Electronic soldering iron

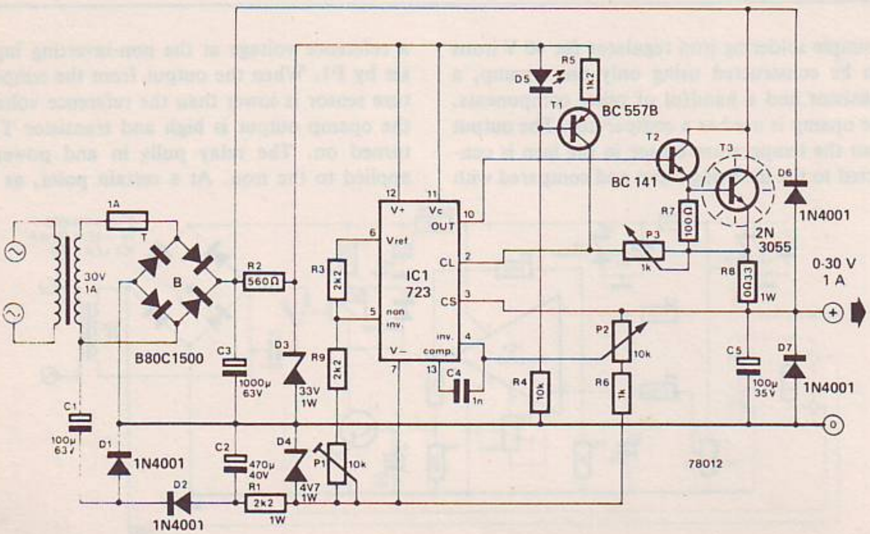
A simple soldering iron regulator for 40 V irons can be constructed using only one opamp, a transistor and a handful of other components. The opamp is used as a comparator. The output from the temperature sensor in the iron is connected to the inverting input and compared with a reference voltage at the non-inverting input, set by P1. When the output from the temperature sensor is lower than the reference voltage, the opamp output is high and transistor T1 is turned on. The relay pulls in and power is applied to the iron. At a certain point, as the



iron heats up, the output from the temperature sensor will exceed the reference voltage causing the opamp output to swing negative, turning off T1.
R6 introduces hysteresis to avoid relay ‘chatter’. D1 and D2 are included to stabilise the reference voltage.
The calibration procedure is relatively simple. Most temperature sensors used in 40 V irons have a sensitivity of 5 mV/100°C. P1 is initially set to maximum. When power is applied, the relay will pull in. The output from the temperature sensor can be monitored with a mV-meter, and P2 is then set so that the relay drops out when this voltage reaches 20 mV, corresponding to 400°C. Alternatively, P2 can be set so that the relay drops out soon after the iron has heated up to the point where solder is melted readily.

44 0 - 30 V regulated supply

This laboratory power supply offers excellent line and load regulation and an output voltage continuously variable from 0 to 30 V at output currents up to one amp. The output is current limited and protected against output fault conditions such as reverse voltage or overvoltage applied to the output terminals. The circuit is based on the wellknown 723 IC regulator. As readers who have used this IC will know, the minimum output voltage normally obtainable from this IC is +2 V relative to the V− terminal of the device (which is normally connected to 0 V). The problem can be overcome by connecting the V− pin to a negative potential of at least −2 V, so that the output voltage can swing down to +2 V relative to this, i.e. to zero volts. To avoid the necessity for a transformer with multiple secondary windings the auxiliary negative supply is obtained using a voltage doubler arrangement comprising C1, C2, D1 and D2 and is stabilised at −4.7 V by R1 and D4. The use of −4.7 V rather than −2 V means that the differential amplifier in the 723 is still operating well within its common-mode range even when the output voltage is zero.
The main positive supply voltage is obtained from the transformer via bridge rectifier B1 and reservoir capacitor C3. The supply to the 723 is stabilised at 33 V by D3 to prevent its maximum supply rating being exceeded and a Darlington pair T2/T3 boosts the output current capability to 1 A. The current limit is continuously variable by means of P3.
The output voltage may be adjusted using P2, while preset P1 is used to set zero output voltage. The supply is protected against reverse polarity



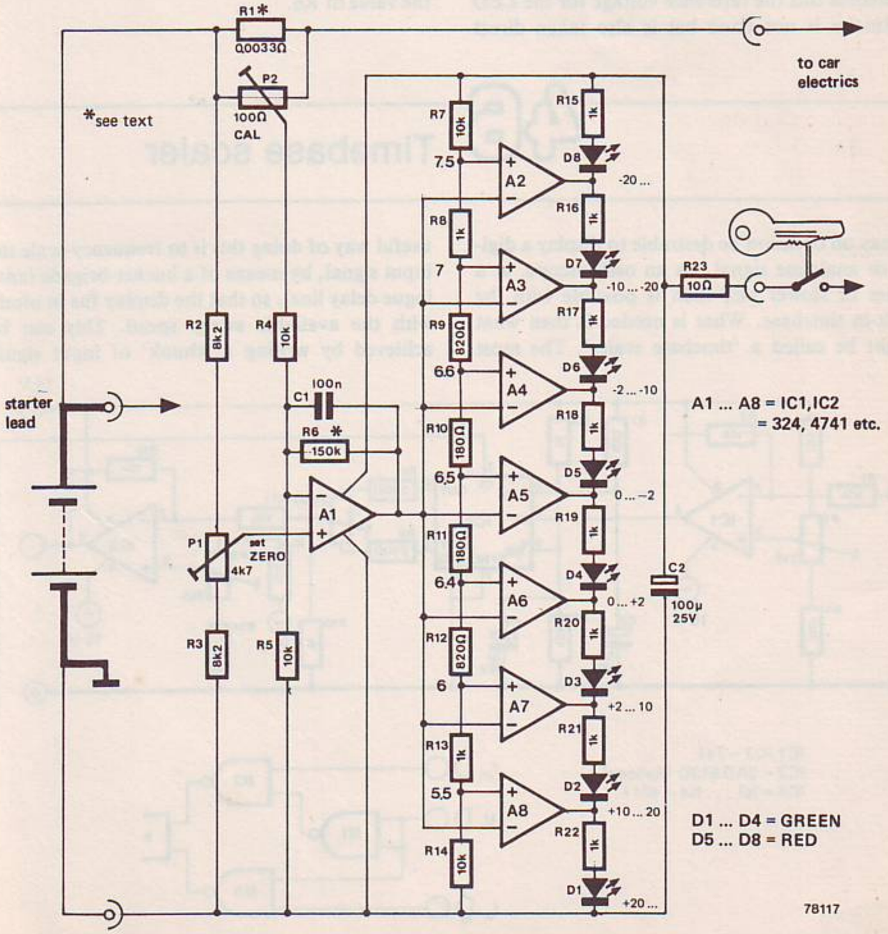
being applied to the output terminals by D7, and against overvoltages up to 63 V by D6.

To set the output voltage to zero P2 is first turned anticlockwise (wiper towards R8) and P1 is then adjusted until the output voltage is zero. With P2 turned fully clockwise the output voltage should then be approximately 30 V. If, due to component tolerance, the maximum output is less than 30 V the value of R6 may require slight reduction. When constructing the circuit particular care should be taken to ensure that the 0 V rail is of low resistance (heavy gauge wire or wide p.c.b. track) as voltage drops along this line can cause poor regulation and ripple at the output.

45 Car ammeter

A surfeit of circuits has already been published for solid-state car battery voltage monitors. However, no design for a corresponding car ammeter has so far appeared. This design remedies that omission.

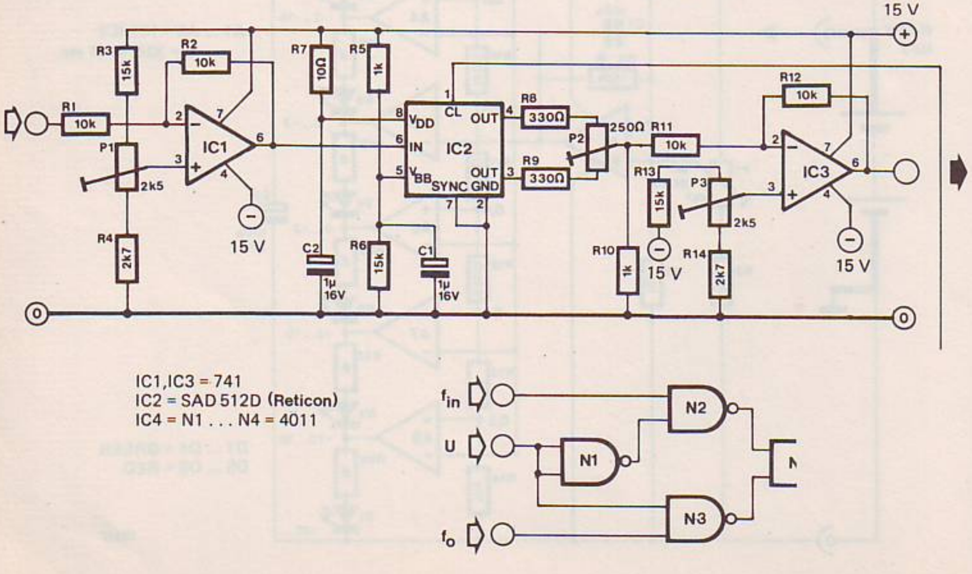
Resistor R1 is a shunt across which is a voltage



proportional to the current flowing through it (max 133 mV at 40 A). The voltage drop across this shunt is amplified by differential amplifier A1 and used to drive a LED voltmeter comprising A2 to A8. With no current through the shunt, P1 is used to set the output voltage of A1 to nominally 6.5 V, so that the circuit is just on the point of switching over from D4 to D5.
When current is drawn from the battery, the right-hand end of the shunt will be at a lower potential than the left-hand end, so the output of A1 will rise, and the discharge indicating LEDs D5 to D8 will light successively as the current increases. When current flows into the battery, the converse is true, the output of A1 falls, and the charge indicating LEDs D4 to D1 light successively. Of course, variation in battery voltage will also cause the output voltage of A1 to rise and fall, which could give false readings. To overcome this the reference voltage for the LED voltmeter is not fixed but is also taken direct from the battery, so that it rises and falls with the output of A1. This does mean that the calibration of the meter varies slightly with battery voltage, but extreme precision is not a prerequisite for a car ammeter. With the component values shown the calibration is nominally correct at a battery voltage of 13 V, but may vary by ± 15% if the battery voltage changes between 11 V and 15 V.
Several possibilities exist for R1. It can be wound using Manganin or Eureka resistance wire; alternatively the voltage drop along the lead between the battery and regulator box may be utilised by connecting one end of P2 to the positive battery terminal and the other end to the battery lead at the regulator box. P2 can then be used to calibrate the ammeter. If the voltage drop along the battery lead is insufficient it may be necessary to raise the gain of A1 by increasing the value of R6.

46 Timebase scaler

It may on occasion be desirable to display a digital or analogue signal, on an oscilloscope, at a faster or slower rate than is possible with the built-in timebase. What is needed is then what might be called a 'timebase scaler'. The most useful way of doing this is to frequency-scale the input signal, by means of a bucket-brigade (analogue delay line), so that the display fits in nicely with the available sweep speed. This can be achieved by writing a 'chunk' of input signal



into the memory 'buckets' at one clock rate, then reading the same chunk out at a lower or higher rate.

The simple circuit shown here will process analogue and digital signals up to 200 kHz. The total write-read cycle should not last longer than 0.1 s (at normal temperatures), otherwise too much information will be lost in the leaky buckets, giving an unacceptably attenuated output. The actual bucket brigade (IC2, Reticon type SAD 512) is preceded and followed by DC-level shifters using 741's. If the DC signal component is not of interest, the level-restorer (IC3) can be omitted and the signal taken out directly through a 100 nF capacitor.

When the control voltage U is *low,* the 'writing' clock frequency f_{in} is fed to the bucket brigade; when U is *high* the 'read' clock frequency (f_o) is applied. During the write-phase there will in general also be an (unwanted) output signal; it may be desirable to also arrange to suppress the output when U is low. If the circuit is to process a periodic signal, the control voltage should be obtained from a trigger running on the input signal, otherwise each chunk of output signal will start with a different phase. It will also be necessary to generate a number of write-periods per chunk at least equal to the number of buckets (512), to prevent 'old' information being read out.

The circuit given contains three preset potentiometers. Start by setting P1 to bring the output of IC1 to about 5 volts. Then set P2 for minimum clock noise on the output signal. Now slightly readjust P1 to achieve symmetrical clipping of an excessive signal. Finally set P3 to give the required output DC level, preferably by setting the output to 0 volts with the circuit input shorted to earth.

47 Model railway lighting

Generally speaking, the internal lighting for model railway carriages is powered direct from the voltage on the rails. However, this voltage is also used to power the locomotive and is varied to control the speed of the train. The result is that the brightness of the lighting varies with the speed of the train, and if the train is actually stopped, then the lighting will be completely extinguished. It goes without saying that such an arrangement involves a complete loss of realism. However, this problem can be resolved with the aid of the following circuit which ensures an independent supply for the carriage lighting.

The circuit utilises the fact that a DC motor will not operate off an AC supply, and that, furthermore, has a fairly high impedance if the frequency of the AC voltage is high enough. This means that if a high-frequency AC voltage is super-imposed upon the normal (DC) supply voltage for the locomotive, it will have no effect upon the speed of the train, but it can be used to power the carriage lighting. To ensure that the lighting is supplied solely by the AC voltage, each carriage is DC decoupled by means of a capacitor.

The principle behind the circuit is illustrated in figure 1. The inductor, L, prevents AC voltages from getting back into the DC power supply. Since this coil has to be able to withstand fairly large DC currents, it would be a good idea to use

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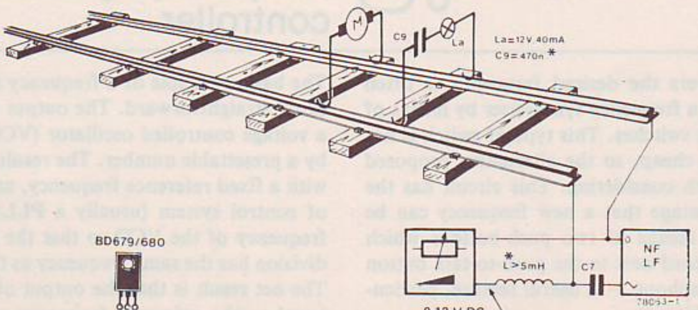

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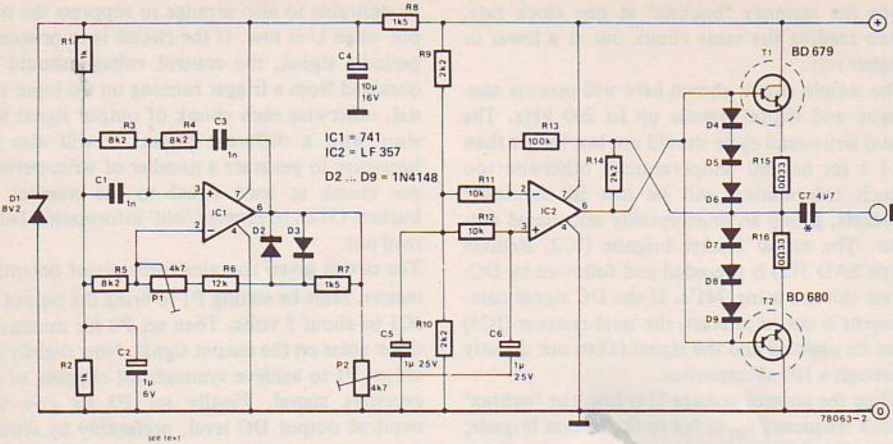
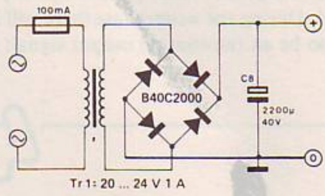




the type of coil employed in loudspeaker cross-over filters.

Figure 2 shows the circuit diagram of the circuit used to supply the necessary AC voltage. The circuit actually consists of a sinewave generator followed by an amplifier which can deliver a current of approx. 1.5 A for a maximum output voltage of 10 V RMS, i.e. sufficient to supply roughly 30 lamps. The frequency of the sinewave generator round IC1 is approx. 20 kHz. The gain of IC1 is adjusted by means of P1 until a pure sinewave is obtained at the output of the IC. The amplitude of the output voltage is set by means of P2. The best results are obtained when P2 is adjusted such that, under maximum load condition (approx. 30 lamps), the output voltage exhibits minimum distortion. A polyester or polycarbonate (e.g. MKH) capacitor should be used for C7. If the value shown should prove unobtainable in a single capacitor, then several MKH (MKM) capacitors can be connected in parallel. Since they cannot withstand large AC currents, the use of bipolar electrolytics is unsatisfactory. For every carriage lamp a series capacitance of about 0.5 µ is required. Thus, if the carriage lighting consists of two lamps, then the capacitor in series with these two lamps should have a value of approx. 1 µF. Again, the use of MKH or MKM capacitors is recommended. Finally, it should be noted that the output of the circuit is short-circuit proof, and that transistors T1 and T2 should be provided with heat sinks.

48 Frequency synthesiser controller

In transceivers the desired frequency is often dialled into a frequency synthesiser by means of thumbwheel switches. This type of switch is not particularly cheap, so the alternative proposed here is worth considering. This circuit has the added advantage that a new frequency can be selected by means of two push-buttons which can be mounted next to the push-to-talk button on the microphone – a useful feature, particularly for mobile use.

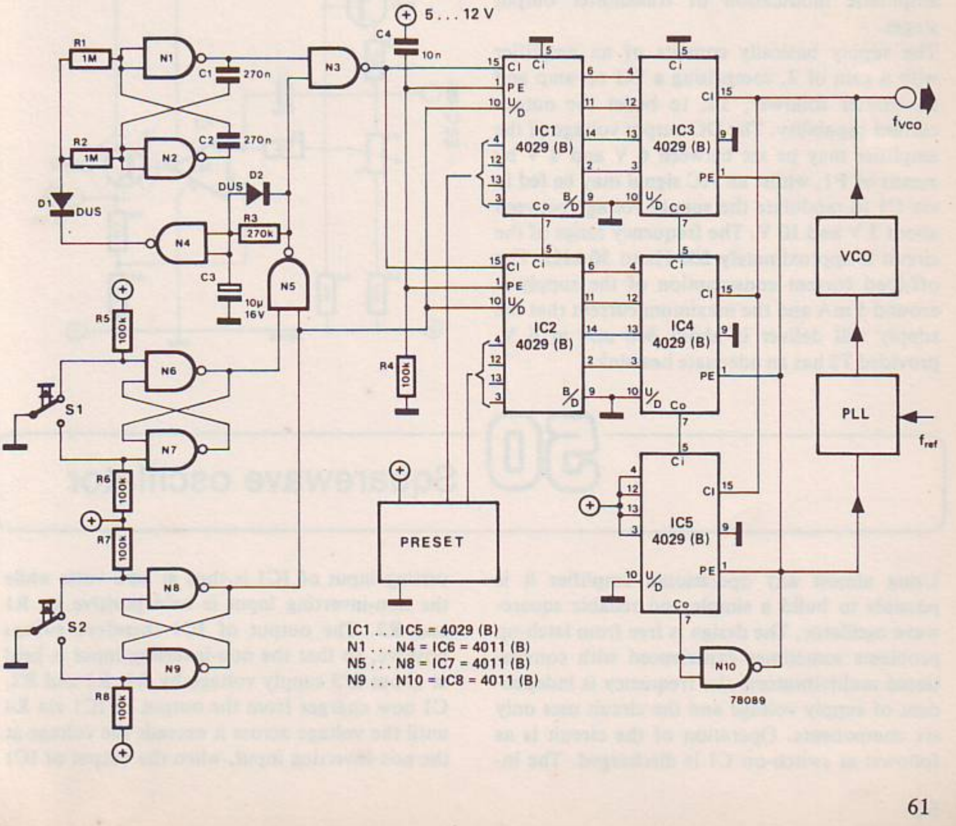
The basic principle of a frequency synthesiser is fairly straightforward. The output frequency of a voltage controlled oscillator (VCO) is divided by a presettable number. The result is compared with a fixed reference frequency, and some type of control system (usually a PLL) adjusts the frequency of the VCO so that the result of the division has the same frequency as the reference. The net result is that the output of the VCO is equal to the reference frequency multiplied by

the division ratio, so that it can be easily and accurately tuned in a succession of fixed steps by altering this division ratio.

In the circuit described here, the VCO output (f_{VCO}) is divided by IC3, IC4 and IC5. These counters are set in the decimal down-count mode. Each time they reach zero (000) the carry-out pulse of IC5 is fed through N10 to the preset-enable inputs of these three ICs. IC3 and IC4 are then preset to the decimal number determined by two further divide-by-ten counters, IC1 and IC2, and IC5 is preset to 1111. The same pulse is fed to one input of the PLL, where it is compared with the reference frequency. The output frequency of the pulses from N10 must therefore be equal to the reference frequency and, since the VCO output is used to clock the counters, the output frequency of the VCO must therefore be equal to the reference frequency multiplied by a number '9XY', where X and Y are the 'preset' values stored in IC2 and IC1 respectively. As an example, if the reference frequency is 1 kHz the tuning range will be from 900 to 999 kHz in 1 kHz steps. If the preset number in IC1 is 4 and the number in IC2 is 6, the output frequency in this case will be 964 kHz.

If IC1 and IC2 where thumbwheel switches, the circuit would be fairly conventional. However, they aren't. As noted earlier, these ICs are decimal counters and they will only 'store' a number as long as they do not receive count pulses. S1 and S2 are used to set up the required count, S1 causing them to count up and S2 resulting in count-down. If either of these buttons is pressed briefly, the count will change by one. However, if the button is held down the count will continue to change in the direction determined by the choice of pushbutton (S1 increasing the count and S2 decreasing it), whereby the rate at which new values occur increases if the button is held down for any length of time.

Starting from the pushbuttons, this part of the circuit operates as follows. N6 and N7 suppress contact bounce for S1; similarly N8 and N9 clean up the output from S2. When either of the buttons is operated the corresponding output (from N6 or N8) goes low, so the output of N5 goes high and N3 is enabled. This gate will now pass the output of the voltage-controlled square-wave generator, consisting of N1 and N2, to the



clock inputs of IC1 and IC2. The clock frequency from N1 and N2 depends on the output state of N4: If this output is high the clock frequency is low and vice versa.

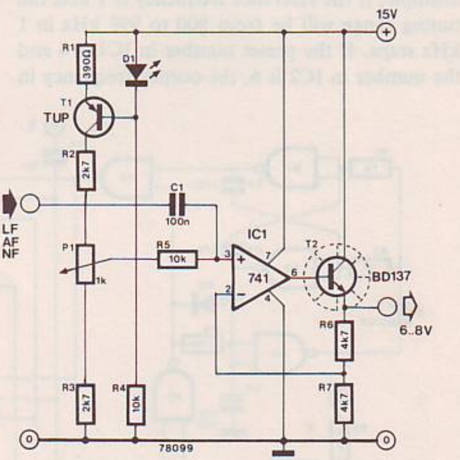
Initially, C3 is discharged, the output of N4 is high, and the clock frequency is low. However, if a pushbutton is held down the output of N5 will remain high, charging C3 through R3. After a short time C3 will have charged sufficiently for the output of N4 to change state and the clock frequency will increase. As soon as the button is released C3 will discharge rapidly through D2 and N5. When S1 is operated, the output of N6 is low and the output of N8 is high, so IC1 and IC2 are in the up-count mode. When S2 is operated, the output of N6 is high but the output of N8 is low; this output state switches both counters into the down-count mode.

Both IC1 and IC2 can be preset at initial switch-on of the circuit. To this end C4 and R4 are included; these components enable the preset inputs of these counters briefly when power is first applied. Any desired initial setting can be programmed (in BCD) by connecting the preset inputs of IC1 and IC2 to positive supply or supply common. This possibility is symbolised in the circuit by the rectangle labelled 'preset'.

49 Modulatable power supply

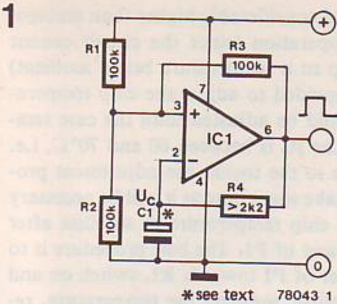
This DC power supply, whose output voltage can be modulated by an audio-frequency or other LF signal, is intended for such applications as modulation of Gunn-diode oscillators and amplitude modulation of transmitter output stages.

The supply basically consists of an amplifier with a gain of 2, comprising a 741 op-amp and an emitter follower, T2, to boost the output current capability. The DC output voltage of the amplifier may be set between 6 V and 8 V by means of P1, whilst an AC signal may be fed in via C1 to modulate the supply voltage between about 3 V and 10 V. The frequency range of the circuit is approximately 200 Hz to 30 kHz. The off-load current consumption of the supply is around 5 mA and the maximum current that the supply will deliver is about 800 mA at 6 V, provided T2 has an adequate heatsink.



50 Squarewave oscillator

Using almost any operational amplifier it is possible to build a simple and reliable squarewave oscillator. The design is free from latch-up problems sometimes experienced with conventional multivibrators, the frequency is independent of supply voltage and the circuit uses only six components. Operation of the circuit is as follows: at switch-on C1 is discharged. The inverting input of IC1 is thus at zero volts while the non-inverting input is held positive by R1 and R2. The output of IC1 therefore swings positive, so that the non-inverting input is held at about 2/3 supply voltage by R1, R2 and R3. C1 now charges from the output of IC1 via R4 until the voltage across it exceeds the voltage at the non-inverting input, when the output of IC1



swings down to about zero volts. The exact positive- and negative-going output swing achieved depends on the type of opamp used. The non-inverting input of IC1 is now at 1/3 supply voltage.

C1 now discharges through R4 into the output of IC1 until its voltage falls below that on the non-inverting input, when the output of IC1 again swings positive and the cycle repeats. Since variations in supply voltage equally affect the charging of C1 and the threshold levels at which the opamp output changes state, these two effects cancel and the oscillation frequency is independent of supply voltage.

The frequency of oscillation is given

$$\text{by } f = \frac{1}{(1.4)\ R_4 C_1}$$

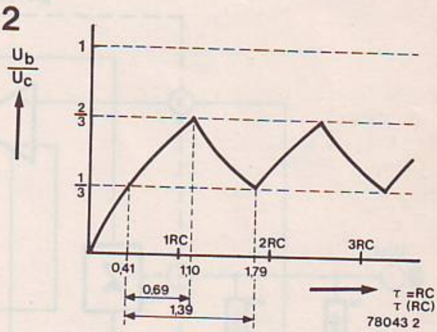
where f is in Hertz
R4 is in Ohms
C1 is in Farads

Alternatively, if R4 is in kilohms and C1 is in microfarads then f will be in kilohertz.

Practically any opamp may be used in this circuit and table 1 lists several popular opamps, together with the supply voltage range over which each may be used and the maximum oscillation frequency which is typically obtainable. The duty-cycle of the squarewave should be

Table 1.

Op-amp	lowest supply voltage	highest supply voltage	highest frequency
709	5 V	36 V	325 kHz
741	3.5 V	36 V	100 kHz (triangular output above 30 kHz due to slew-rate limiting)
CA3130	3 V	16 V	275 kHz
CA3140	5 V	36 V	200 kHz
CA3100	8.5 V	36 V	275 kHz
LF357	3 V	36 V	325 kHz
LM301	3 V	36 V	325 kHz



50%, but due to slight asymmetry in the output stages of the opamps this will not be the case. The only opamp amongst those listed which will give a duty-cycle of exactly 50% is the CA 3130. At low supply voltages it may also be found that the frequency changes with supply voltage due to variations in the output characteristics of the opamps. However, with supply voltages greater than 10 V this should not be a problem.

The working voltage of C1 must be at least 2/3 of the supply voltage.

51 Temperature-compensated

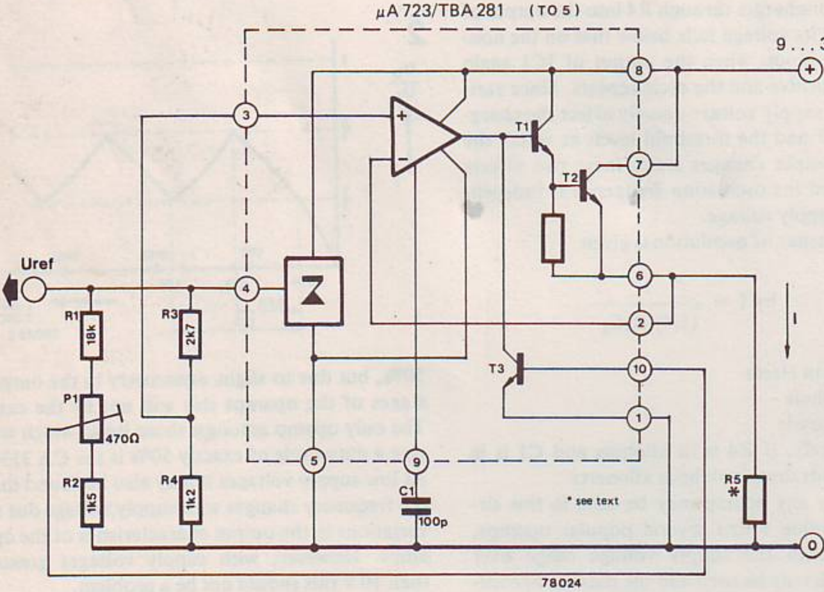
The popular 723 IC regulator has an on-chip reference voltage with a fairly low temperature coefficient. By using a simple gimmick the 723 can be used as an 'oven' to maintain itself (and hence the reference voltage) at a virtually constant temperature, thus practically eliminating the temperature dependence of the reference voltage. The 723 is connected as a unity-gain non-inverting amplifier, to whose input is fed a voltage

$$\frac{U_{ref} \times R_4}{R_3 + R_4}$$

This causes a current to flow through load resistor R5 via T1 and T2, the output transistors of the 723. The power dissipated in these transistors causes the chip temperature to rise. The temperature of the IC is between 60 and 70°C, i.e. just bearable to the touch. The adjustment procedure may take some time as it will be necessary below the value set by P1 then T3 will turn on, cutting off the output current until the chip temperature has fallen sufficiently for T3 to turn off again.

The result is that the chip, and hence the reference voltage, is held at a virtually constant temperature. Obviously the chip temperature must be maintained considerably higher than ambient for correct operation (since the circuit cannot cool the chip to a temperature below ambient) and P1 is provided to adjust the chip temperature. P1 should be adjusted until the case temperature of the IC is between 60 and 70°C, i.e. just bearable to the touch. the adjustment procedure may take some time as it will be necessary to allow the chip temperature to stabilise after each adjustment of P1. The best procedure is to turn the wiper of P1 towards R1, switch on and allow to stabilise, measure the temperature, readjust P1, allow to stabilise etc.

The value of R5 is dependent on the supply voltage used and should be 33 ohms for voltages between 9 V and 15 V, 68 ohms for 15 V to 25 V and 100 ohms for 25 V to 35 V.

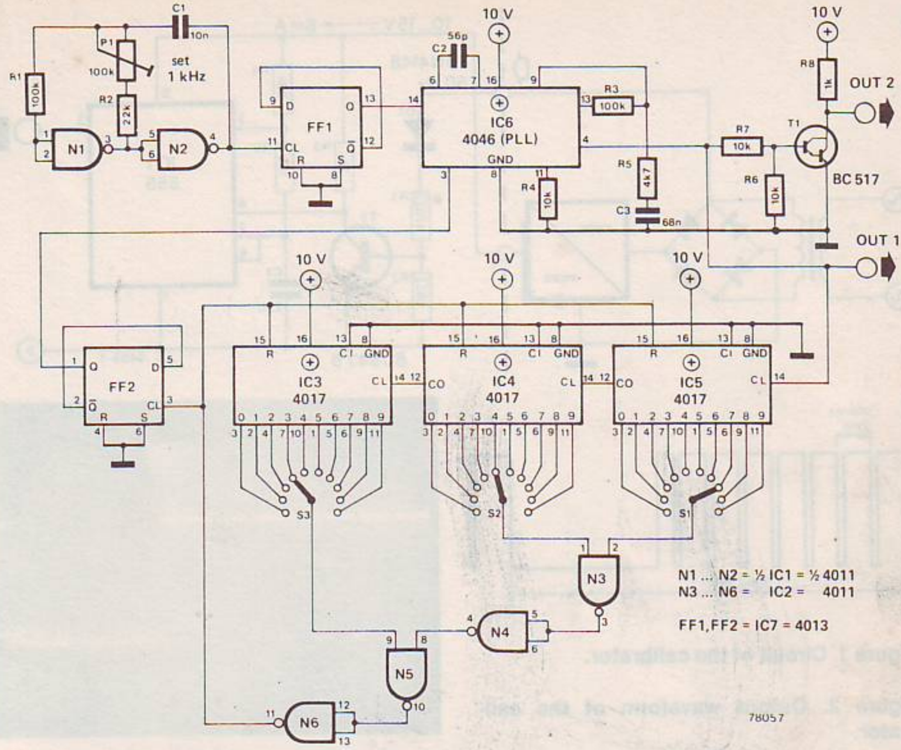


52 Frequency synthesiser

The output frequency of this squarewave generator can be programmed in 1 kHz steps from 1 kHz to 999 kHz. The heart of the circuit is a 4046 CMOS phase-locked loop which has an extremely wide capture range.

The output of a 1 kHz clock generator, N1/N2, is divided down by FF1 to give a symmetrical 500 Hz squarewave output, which is fed to one of the phase comparator inputs of the 4046 (IC6). The Voltage Controlled Oscillator (VCO) output of IC6 is fed to the second input of the phase comparator via a programmable frequency divider (IC3-IC5) and FF2.

The VCO output frequency of the PLL adjusts



itself until the output of FF2 has the same frequency and phase as the clock output from FF1. If the division ratio set on switches S1 to S3 is n then the VCO frequency must obviously be n times the 1 kHz clock frequency. Setting a number n on switches S1 to S3 therefore gives an output frequency of n kHz. The VCO output from pin 4 may be used to drive CMOS circuits direct, however, for other applications a transistor buffer may be required.

If greater frequency accuracy is required then the clock oscillator may be replaced by a more stable 1 kHz reference frequency such as the divide-by-10^3 output of the IC counter timebase described elsewhere in this book.

53 Scope calibrator

It is comforting to believe in the infallible accuracy of one's test instruments, especially when there are no other standards around to contradict them. However, instruments, and particularly complex ones such as oscilloscopes, tend to drift with age, and if more than a year or so old can be highly inaccurate. This simple calibrator will check the gain and bandwidth of the Y amplifiers and attenuators and the frequency calibration of the timebase. It is so compact that it can be built into virtually any oscilloscope, making regular calibration a simple procedure.

Since the Y attenuators and timing capacitors in an oscilloscope are usually fairly stable components most of the drift generally takes place in the X and Y amplifiers and the rest of the timebase circuitry. Thus an oscilloscope will frequently agree with itself between different Y sensitivity and timebase ranges, even though the calibration may be wildly inaccurate with reference to an external standard. Gross discrepancies between ranges usually occur only in the

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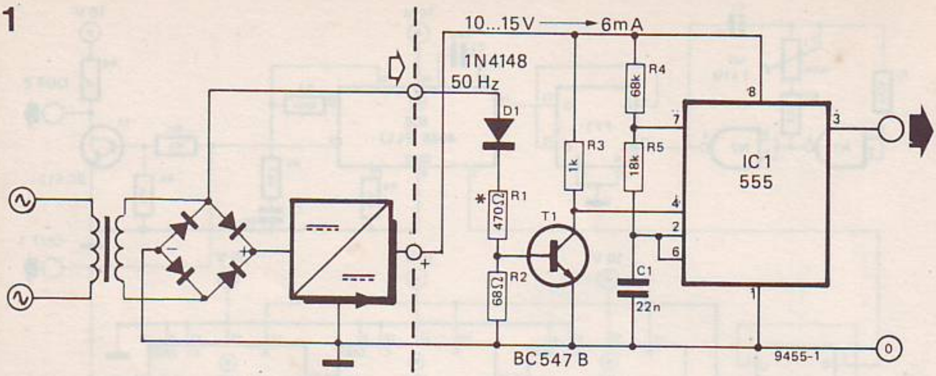

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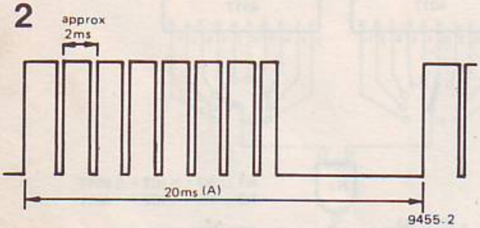

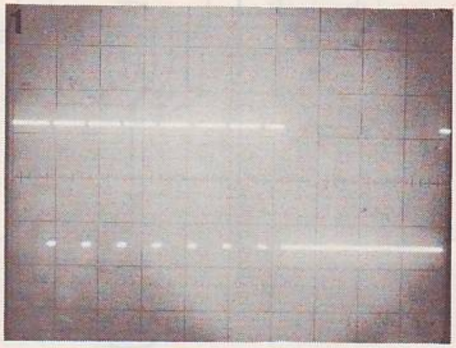

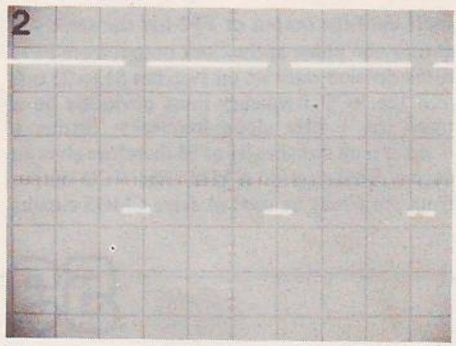

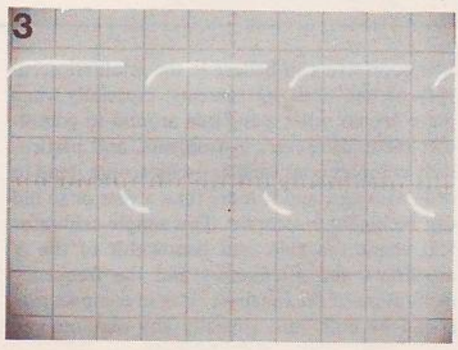

Figure 1. Circuit of the calibrator.

Figure 2. Output waveform of the calibrator.

Figure 3. Printed circuit board and component layout for the calibrator.

Photo 1. Oscillograph of the calibrator output waveform.

Photo 2. An expanded view of a portion of the waveform as seen on a correctly calibrated oscilloscope.

Photo 3. The waveform of photo 2 seen on an oscilloscope with poor h.f. response.

event of a fault in the circuit and a drift in the overall calibration may go unnoticed for some time.

The simple circuit of the calibrator is given in figure 1. It consists of a 555 timer connected as an astable multivibrator with a period of 1.5...2 ms. This is gated on and off by T1, which is driven by a 50 Hz signal. The complete output waveform, shown in figure 2, comprises a burst of pulses (approx. 2 ms) followed by a 10 ms gap, followed by a further burst of pulses and so on. The time from the start of one burst of

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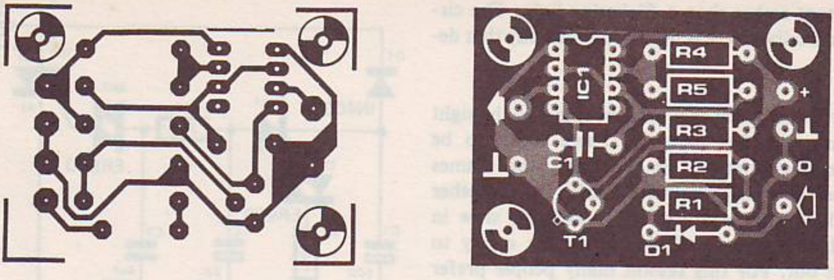


Parts List

Resistors:
R1 = 470 Ω *
R2 = 68 Ω *
R3 = 1 k
R4 = 68 k
R5 = 18 k
* see text

Capacitors:
C1 = 22 n

Semiconductors:
D1 = 1N4148
T1 = BC547B, BC107B
IC1 = 555 timer

pulses to the start of the next burst is equal to the period of the 50 Hz waveform i.e. 20 ms. This can be used to calibrate the oscilloscope timebase. The amplitude of the calibration signal is approximately equal to the supply voltage, which can be measured with a multimeter. The amplitude of the waveform can then be used to calibrate the Y amplifiers.
The 2 ms pulses are useful for checking the bandwidth of the Y amplifiers and the compensation of the Y attenuators and also for calibrating oscilloscope probes. Photo 1 shows an oscillograph of the complete test waveform, while photo 2 shows the pulses as seen on a correctly calibrated oscilloscope. Photo 3 shows the effect of poor highfrequency response due to incorrect adjustment of the compensation trimmers in the Y attenuator.

Construction

A printed circuit board and component layout for the calibrator are given in figure 3. This is very compact and can easily be mounted inside most oscilloscopes. It is assumed that the necessary supply voltage can be derived from the oscilloscope power supplies. With modern transistor oscilloscopes this should be no problem, the supply can probably be derived from one of the low-voltage supplies in the oscilloscope either direct or via a simple zener stabilizer.
The anode of D1 is simply connected to one of the low voltage secondaries of the oscilloscope mains transformer. The values of R1 and R2 depend on the secondary voltage: R1 = 470 Ω up to 8 V; R1 = 680 Ω from 8 V to 11 V; R1 = 1 k from 11 V to 16 V; R1 = 1k5 from 16 V to 23 V; R1 = 3k9/½ W and R2 = 150 Ω from 23 V to 40 V. R2 = 68 Ω, as shown, up to 23 V.
Installation in older, valve-type oscilloscopes may pose a problem and it may be preferable to instal a separate power supply for the calibrator using a miniature mains transformer and a simple zener stabilized supply. Care should then be taken that the magnetic field of the transformer does not affect the performance of the oscilloscope.
The output of the calibrator can be brought out to a socket on the front panel of the oscilloscope so that the calibration can easily be checked by inserting a probe into the socket.

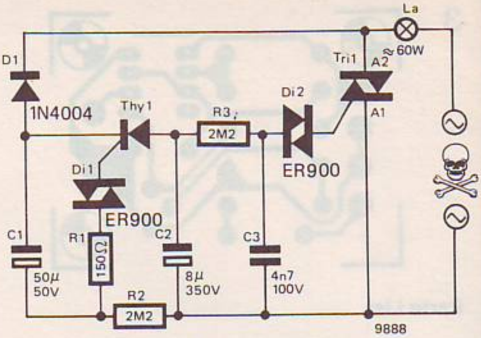
54 Electronic open fire

Many electric fires are equipped with a special coal- or log- effect to simulate the appearance of an open fire. This effect is sometimes spoilt, however, by the fact that the lamp provides a

constant rather than a flickering light. The circuit described here is intended to remedy that defect.

There is no doubt that most people find the sight of an open fire pleasing. There seems to be something soothing in watching the flames flicker and play about the coals. On the other hand, coal fires are difficult to light, slow in producing heat, and also extremely messy to clean out. For this reason many people prefer the convenience and speed of an electric fire, and reluctantly relinquish the pleasures of a hearth fire. Manufacturers of electric fires have realised this fact, and attempted to entice the consumer to buy electric by fitting the front of their fires with a coal- or log effect. Unfortunately, the lamps which are used to illuminate these fronts sometimes provide only a constant light, thereby considerably diminishing the realism of the effect. However, using only a handful of components from the junk-box, it is possible to construct a small circuit to restore the 'flicker' in your fire.

The way the circuit functions is quite simple. When power is applied capacitor C1 is charged via the lamp, resistor R2 and diode D1. After several half cycles of the mains supply, the voltage across this capacitor exceeds the trigger voltage of diac Di1. This diac in turn triggers thryristor Th1, with the result that capacitor C2 charges up rapidly through this thyristor and D1. However, when the mains voltage next crosses zero, this thyristor turns off. Capacitor C3, which is part of the trigger circuit of Tri1, is now charged rapidly by capacitor C2 via resistor R3. This 'DC bias' on C3 decreases as capacitor



Thy1 = Thyristor, 400 V/1 A

Tri 1 = Triac, 400 V/4 A

C2 discharges. This in turn results in a gradual change in the triggering angle of the triac, causing the lamp La to flicker. Once C1 has again reached the trigger voltage of the diac, the entire cycle repeats itself.

As far as component values are concerned, care should be taken to ensure that the maximum current taken by the triac is at least twice the maximum current drawn by the lamp La. For a normal sized fire a 4 A type should prove sufficient. The triac must also be able to withstand the peak mains voltage i.e. approx. 400 V. A 400 V (1 A) thyristor should also prove suitable. D1 may be any commonly available 600 V rectifier diode.

During construction it should be remembered that the full mains voltage may appear across any point in the circuit. For this reason it should be well insulated.

S. Kaul

55 Common-base virtual-earth mixer

The most usual form of virtual-earth mixer consists of an inverting amplifier with the inputs to be mixed (or more accurately summed) being fed via resistors to the virtual-earth point at the inverting input. However this unusual circuit utilises a single transistor operated in common-base configuration, and does not invert the input signals.

T1 receives a constant base bias voltage from R1, D1 and D2, and thus the emitter voltage is also held constant at about 0.6 V. A constant current of $\frac{0.6}{R2}$ thus flows through R2. Assuming, for simplicity, that the mixer is dealing with AC input signals, under quiescent (no signal) conditions the DC current through R2 is almost entirely supplied by T1 and is almost equal to the collector current.

If an AC signal is applied to one of the input resistors R5 then an AC current $\frac{U_n}{R5}$ will flow

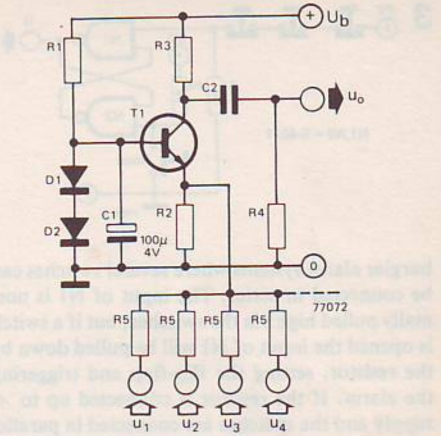
through R2. Since the total current through R2 remains constant the proportion of that current supplied by T1 will vary in sympathy with the input signal and an AC output signal will appear at the collector of T1. The gain of the mixer is $\frac{R3}{R5}$ so, assuming all the R5's are the same, the output voltage $U_0 = \frac{R3}{R5}(U_1 + U_2 + U_3 + \ldots\ldots + U_n)$.

As the emitter of T1 remains at constant voltage it is an almost perfect virtual-earth summing point. The distortion factor of the mixer is determined almost exclusively by the linearity of the current gain in the common-base configuration, which is $\frac{hfe}{1 + hfe}$.

If a high-gain transistor (large h_{fe}) is used then the current gain will be almost unity and variations in h_{fe} will have little effect, so the distortion will be low.

The input resistance of the circuit is equal to R5, so R5 must obviously be made equal to the desired input resistance. R3 is chosen equal to $\frac{R5}{n}$, where n is the number of inputs.

Finally, for optimum results R2 should be made



equal to $\frac{1.2 \times R3}{U_b}$. This fixes the DC collector current of T1 and sets the collector voltage to around half supply.

As an example, if R5 is 33 k and there are four inputs the value of R3 is 8k2. With a supply voltage of 15 V R2 is thus 680 Ω (these are nearest preferred resistors to actual values).

56 CMOS alarm circuits

Because of their low cost, high input resistance, good noise immunity and wide supply voltage range CMOS logic circuits lend themselves to the construction of cheap and reliable alarm circuits for various applications.

Figure 1 shows a basic alarm oscillator constructed around two CMOS NAND gates. As long as input Q is low the circuit remains inactive. When input Q goes high the circuit begins to oscillate, switching T1 and T2 on and off and producing an alarm signal from the loudspeaker.

Figure 2 shows a circuit for triggering the alarm after a preset time delay that can be varied between one second and one minute. On switch-on the input of N2 is briefly held low by C2, so the flip-flop is reset and the Q output is low. C1 now charges via P1 so that the input voltage of N1 falls until the flip-flop is set and the Q output goes high.

Figure 3 is an alarm circuit that is triggered when a circuit is broken, this is particularly useful in

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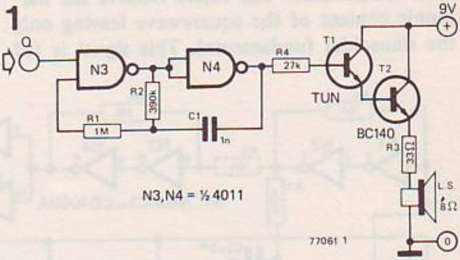

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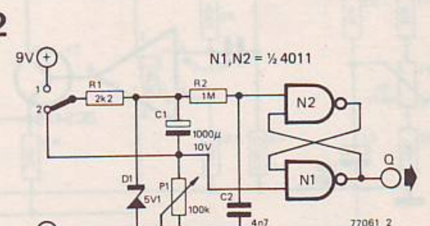

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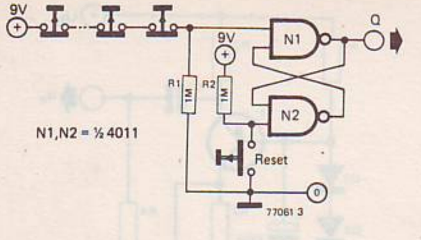

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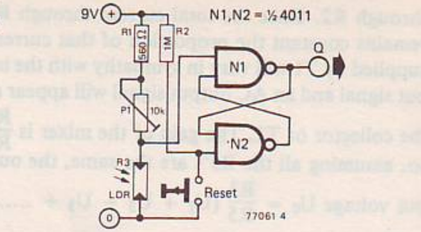


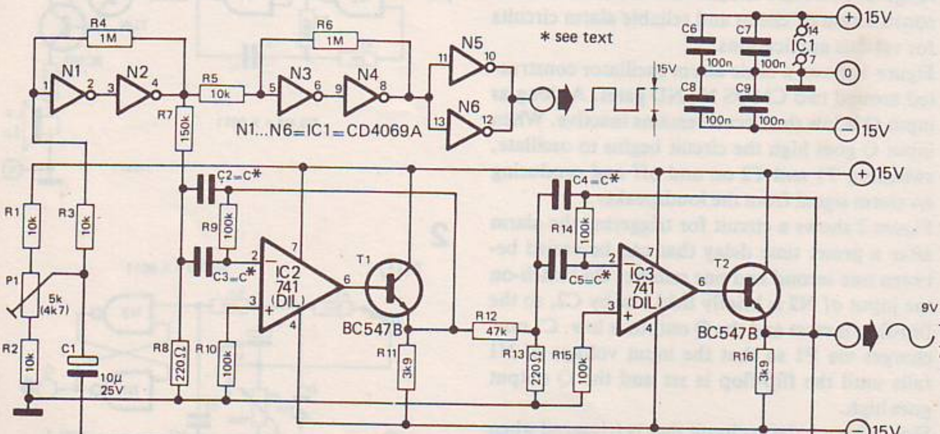
burglar alarm systems where several switches can be connected in series. The input of N1 is normally pulled high via the switches, but if a switch is opened the input of N1 will be pulled down by the resistor, setting the flip-flop and triggering the alarm. If the resistor is connected up to + supply and the switches are connected in parallel down to ground then the alarm can be triggered by closing a switch.

Figure 4 shows an alarm circuit that responds to light. In darkness the resistance of the LDR is high and the input of N1 is pulled high by R1 and P1. If light falls on the LDR the resistance falls and the input of N1 is pulled down, setting the flip-flop and triggering the alarm.

57 Spot-frequency sinewave generator

This circuit employs an unusual method of producing a sinewave signal and, unlike most sinewave generators, requires no amplitude stabilising components such as thermistors or FETs. N1 and N2 are connected as a Schmitt trigger at whose output appears a squarewave (how this happens will become apparent). The squarewave signal is fed into two cascaded selective filters consisting of IC2/T1, IC3/T2 and their associated components. The filters remove the harmonic content of the squarewave leaving only the sinusoidal fundamental. This signal is fed back via C1 to the input of the Schmitt trigger. At each zero-crossing of the sinewave the Schmitt trigger changes state, thus producing the original squarewave that is fed to the input of IC2. P1 adjusts the trigger point of the Schmitt trigger, which varies the duty-cycle of the squarewave and hence the sinewave purity. By suitable adjustment of P1 distortion levels of 0.15% to 0.2% can be achieved. With the ICs used lower figures are not possible due to the distortion introduced by IC3 and T2.

N3 and N4 also function as a Schmitt trigger,



which further speeds up the leading and trailing edges of the squarewave from N2. A squarewave signal with short rise and fall times, synchronised to the sinewave signal, is available at the outputs of N5 and N6. The value of C for a particular frequency f_0 is given by $C\ (\mu F) = \frac{0.34}{f_0\ (Hz)}$.

58 Signal injector

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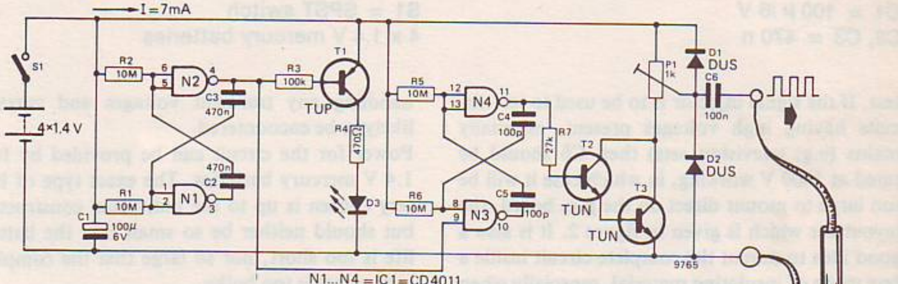

Many people consider the use of signal injectors to be something of a 'brute force' method of faultfinding. However, a signal injector can easily be carried around in the pocket and is often the service engineer's 'first line of defence' when undertaking repairs in the customer's home. Certainly a signal injector is much more portable than an array of sophisticated signal generators.

Most of the cheap signal injectors on the market produce a squarewave output at about 1 kHz. Since the squarewave is rich in harmonics extending up into the Megahertz region these are useful for testing r.f. circuits, as well as using the fundamental for audio testing.

The signal generator described here differs slightly in that the 1 kHz squarewave is keyed on and off at about 0.2 Hz, which makes it easier to trace.

Figure 1 shows the complete circuit of the signal injector. The keying oscillator consists of an astable multivibrator built around two CMOS NAND gates N1 and N2. This switches on and off T1, which drives a LED to indicate when the signal is on. The 1 kHz squarewave generator also consists of an astable multivibrator, which utilises the two remaining NAND gates in the 4011 package. This astable is gated on and off by the first astable. The output of the 1 kHz oscillator is buffered by transistors T2 and T3, the output being taken from the collector of T3 via a potentiometer P1 which serves to adjust the output level. The maximum output is approximately equal to the supply voltage (5.6 V). Diodes D1 and D2 provide some protection for T2 and T3 from external transients, and C6 isolates the circuit from any DC voltage in the circuit under

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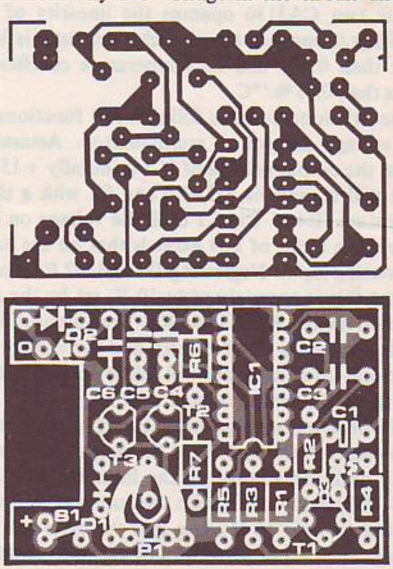


Parts List

Resistors:
R1, R2, R5, R6 = 10 M
R3 = 100 k
R4 = 470 Ω
R7 = 27 k
P1 = 1 k preset

Capacitors:
C1 = 100 µ/6 V
C2, C3 = 470 n
C4, C5 = 100 p
C6 = 100 n/250 V (see text)

Semiconductors:
IC1 = 4011
T1 = TUP
T2, T3 = TUN
D1, D2 = DUS (see text)
D3 = LED (e.g. TIL209)

Miscellaneous:
S1 = SPST switch
4 x 1.4 V mercury batteries

test. If the signal injector is to be used to test circuits having high voltages present, especially mains (e.g. television sets) then C6 should be rated at 1000 V working, in which case it will be too large to mount direct on the p.c. board, the layout for which is given in figure 2. It is also a good idea to mount the complete circuit inside a box made of insulating material, especially when working on live chassis equipment such as a television set. D1 and D2 should be types capable of handling any transient voltages and currents likely to be encountered.
Power for the circuit can be provided by four 1.4 V mercury batteries. The exact type of battery chosen is up to the individual constructor, but should neither be so small that the battery life is too short, nor so large that the complete instrument is too bulky.

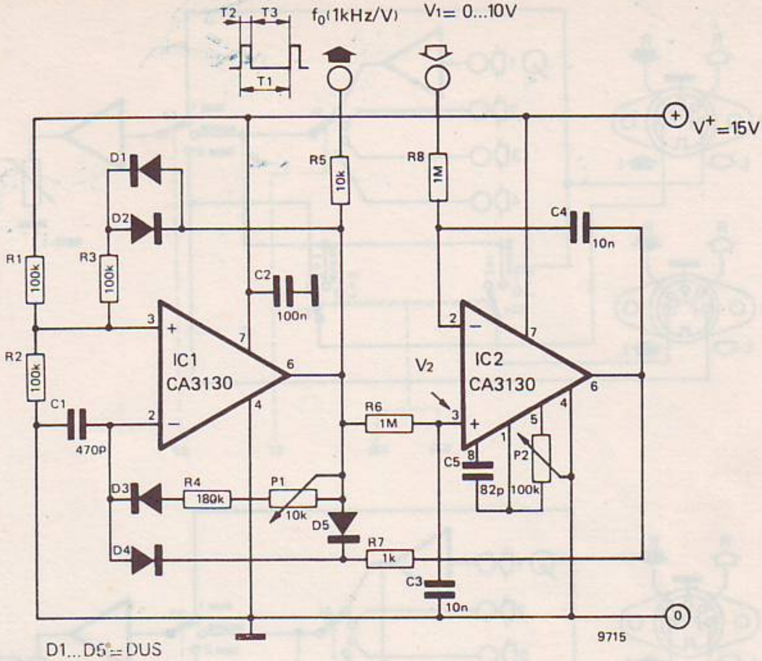
J.W. van Beek

59 Precision V to f converter

Although this Voltage Controlled Oscillator uses only two CA3130 opamps the linearity of its voltage/frequency transfer characteristic is better than 0.5% and its temperature coefficient less than 0.01%/°C.
The circuit operates as follows: IC1 functions as a voltage controlled multivibrator. Assuming that the output voltage of IC1 is initially +15 V, C1 will charge via D3, R4 and P1 with a time constant (R4 + P1) C1 until the voltage on the inverting input of IC1 exceeds that on the non-inverting input. Neglecting D1 and D2 for a moment this is approximately 10 V, set by the potential divider R1, R3 and R2. The output of IC1 will now swing down to zero and the voltage on the non-inverting input will fall to about 5 V due to the hysteresis introduced by R3.
C1 will now discharge into the output of IC2 at a rate determined by R7 and the output voltage of IC2 until the voltage on the inverting input of IC1 falls below 5 V, when the output of IC1 will swing up to +15 V again and the cycle will repeat. The output waveform of IC1 thus consists of a series of positive pulses whose duration (T2) is a constant and whose spacing (T1) depends on the output voltage of IC2.
The output voltage of IC1 is filtered by R6 and C3 to give a DC voltage (V_2) equal to the average value of the IC1 waveform i.e.

$$V_2 = 15 \times \frac{T_2}{T_1}.$$

Since T2 is constant V_2 is proportional to 1/T1 i.e. proportional to the output frequency of IC1.
The input voltage V_1 is applied to the inverting input of IC2, which functions as an integrating comparator. If V_1 is less than V_2 the output of IC2 will ramp positive. C1 will thus discharge at a slower rate, making the interval T1 longer and reducing V_2. If V_1 is greater than V_2 then the output of IC2 will ramp negative (i.e. towards zero) making C1 discharge more quickly and reducing T1. When V_1 and V_2 are equal the output voltage of IC2 will remain constant.
The circuit will thus always reach equilibrium with $V_1 = V_2$. However, since V_2 and the output



frequency of IC1 are proportional then the output frequency of IC1 is also proportional to the input voltage V_1, since V_1 and V_2 are equal.

A few small refinements are added to improve the temperature stability of the circuit. The temperature coefficients of D3 and D4 could introduce errors by varying the charge and discharge times of C1, so these are compensated by including identical diodes in series with R3 to produce a similar variation in the reference voltage at the non-inverting input of IC1.

P2 is included to null the offset voltage of IC2 which would otherwise cause a zero error.

P1 provides fine adjustment of the conversion ratio, which with the values given is about 1 kHz/volt.

Lit.: RCA Application Notes

60 Monitor switching for two tape decks

Although modern audio amplifiers frequently sport an abundance of (seldom-used?) gimmicks, very few amplifiers possess comprehensive tape switching and monitoring facilities. Most have only a single tape socket, with facilities for making a recording onto one tape deck and monitoring that recording, and have no provision for a second tape deck.

The simple switching circuits described here will allow recording from disc or other sources onto two tape recorders, either one at a time or simultaneously, with monitoring of both recordings. In addition, transcription from either tape recorder to the other is possible, while at the same time a totally different source (disc, tuner, etc.) can be played through the amplifier.

The switching circuit is shown in figure 1. The function selector switch of the amplifier (disc, tuner, aux, etc.) is represented by S1. S2 and S3 are part of the switching unit. With S3 in its centre position a signal can be taken from the source to the record inputs of both tape recorders. With S1 in position 1 → 2 the playback output of one tape deck is fed to the record input of the second, while in the 2 → 1 position the playback output of the second deck is fed to the

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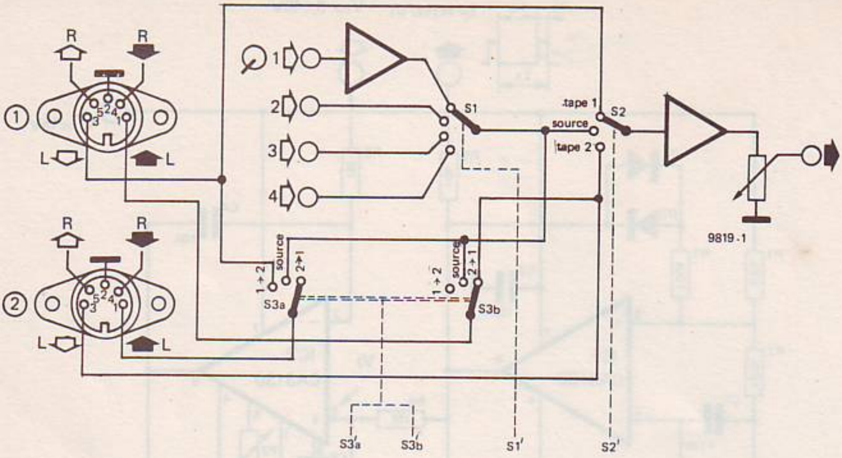

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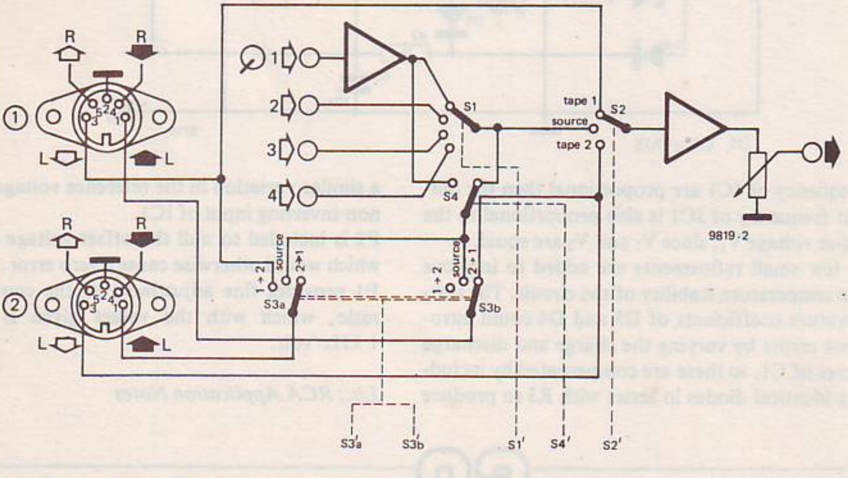

record input of the first.

Whatever the position of S3, monitoring of tape 1, source, or tape 2 is possible by means of S2. Therefore, with S3 in position 1 → 2 or 2 → 1 it is still possible to listen to disc, tuner, etc. by setting S2 to its centre position. For clarity only the left channel is shown, but the right channel is identical.

The circuit may be incorporated into the amplifier by inserting it between the output of the function switch and the input of the next stage of the amplifier. The original tape monitor switch (if fitted) can be discarded and replaced by S2, while an extra hole must be drilled in the front panel for S3.

Alternatively the switching unit can be mounted in its own box and can be connected to the amplifier via the existing tape socket. The output to the unit is simply taken from the record pin of the tape socket, and the input back to the amplifier from the rotor of S2 is taken to the replay pin of the tape socket. The amplifier must then be operated with the tape monitor switch depressed.

A slight modification to the circuit, shown in figure 2, allows recording from disc while listening to a different source. With S4 in the left-hand position the output of the disc preamp can be tapped off and fed to the tape decks, while S1 can be in any of its four positions, thus allowing disc or some other source to be listened to at the same time. The recording may also still be monitored by setting S2 to 'tape 1' or 'tape 2'.

61 AM/FM alignment generator

This circuit can be used to align IF strips with a frequency of 455 kHz. The generator produces a 455 kHz signal which, depending upon the position of switches S1 and S2, is either amplitude- or frequency modulated.

The actual oscillator is built round FET T1. A conventional IF transformer is used to determine the frequency. The alignment generator is tuned to the correct frequency by passing the output signal through a ceramic IF filter. After rectification the signal can be measured on a voltmeter to ascertain at which setting of the IF transformer coil the amplitude of the signal is greatest. The frequency of the generator should then coincide with the desired value of 455 kHz.

The circuit is provided with the possibility of AM and FM modulation. When the generator is being aligned, switch S1 should be open, thereby

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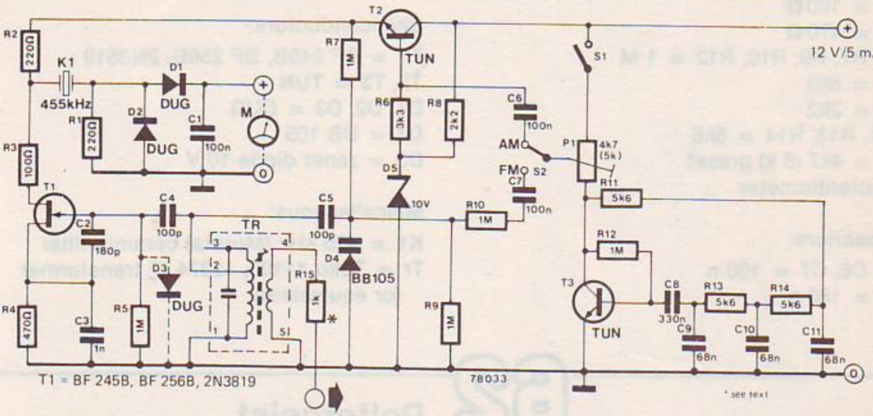

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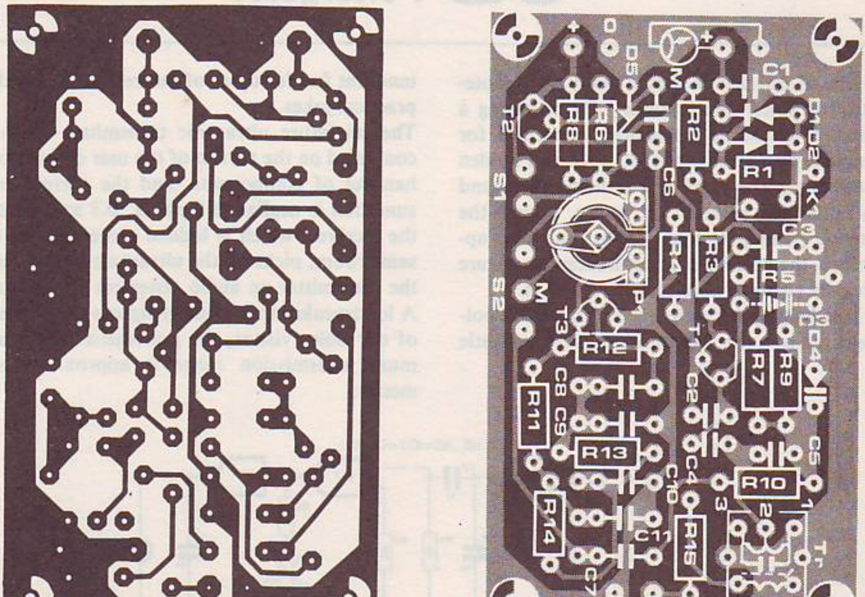

preventing modulation of the output signal. The modulation signal is generated by the low frequency oscillator round T3.
Amplitude modulation is realised by modulating the supply voltage of T1 via T2. S2 should then be in the 'AM' position. Frequency modulation (S2 in the 'FM' position) is obtained by means of the varicap diode, D4. In both cases the modulation depth can be varied by means of P1.
The output signal of the alignment generator is taken from the secondary winding of the IF transformer. Depending upon the desired output voltage and impedance, the series output resistor, R15, can have any value above 100 Ω. In most cases a value of 1 k should prove sufficient.

Parts list

Resistors:
R1, R2 = 220 Ω
R3 = 100 Ω
R4 = 470 Ω
R5, R7, R9, R10, R12 = 1 M
R6 = 3k3
R8 = 2k2
R11, R13, R14 = 5k6
P1 = 4k7 (5 k) preset potentiometer

Capacitors:
C1, C6, C7 = 100 n
C2 = 180 p
C3 = 1 n
C4, C5 = 100 p
C8 = 330 n
C9, C10, C11 = 68 n

Semiconductors:
T1 = BF 245B, BF 256B, 2N3819
T2, T3 = TUN
D1, D2, D3 = DUG
D4 = BB 105
D5 = zener diode 10 V

Miscellaneous:
K1 = 455 kHz (Murata) ceramic filter
Tr = Toko 11100, 12374 IF transformer (or equivalent)

62 Poltergeist

The title of this article should really be 'remote-controlled poltergeist-imitator'. By operating a miniature ultrasonic transmitter concealed for example in one's jacket pocket, a receiver hidden somewhere in the room will simulate the sound of a poltergeist loose in the house. Should the authentic poltergeist then fail to put in an appearance, the ambitious ghost-hunter can ensure success by virtue of his electronic stand-in.
The idea behind this article is not to put the poltergeist out of a job, but rather to provide a little innocent fun for those of our readers inclined to practical jokes.
The miniature ultrasonic transmitter which is concealed on the person of the user consists of a handful of components, and the current consumption is negligible (approx. 0.3 mA). When the receiver, which is hidden somewhere in the same room, picks up the ultrasonic signals from the transmitter an audio generator is activated. A loudspeaker then audibly signals the presence of our noisy visitor, the poltergeist. The maximum transmission range is approx. 4 to 5 metres.

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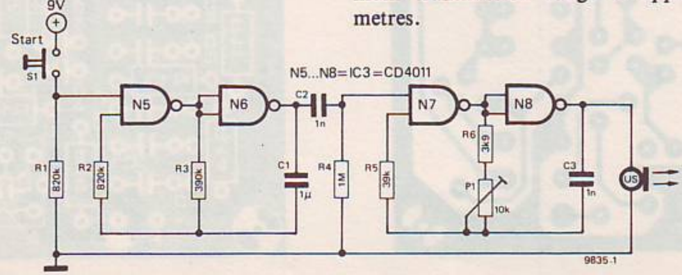

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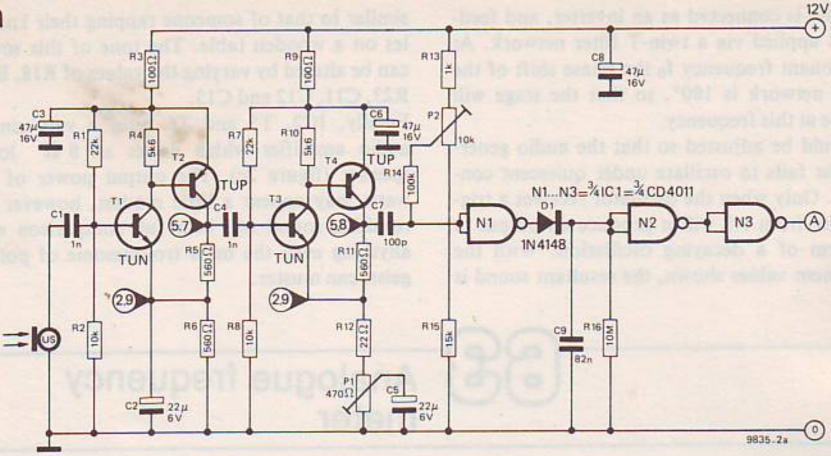


The transmitter

As is apparent from figure 1, the ultrasonic transmitter requires little more than one IC type 4011 and an ultrasonic transducer.

The four gates of the IC are used to form two astable multivibrators; the frequency of the first (N5, N6) is approx. 1 Hz, whilst that of the second (N7, N8) is roughly 40 kHz. Closing S1 starts the first AMV, which triggers the second AMV at 1 second intervals. This second AMV then produces a burst of 40 kHz ultrasonic signal, lasting only a few milliseconds. As a glance at the circuit diagram makes clear, the circuit is ideally suited for miniaturisation; as already mentioned, the current consumption is so small as to be negligible.

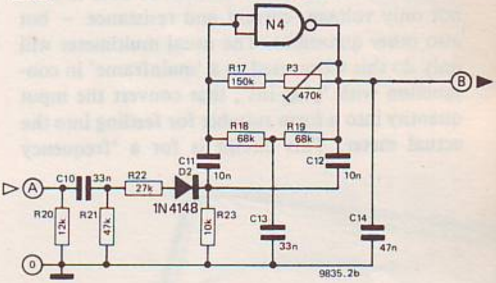
The receiver

Figures 2a, 2b and 2c show the circuit diagram of the receiver. The input signal is fed to a two-stage amplifier, each stage consisting of a pair of DC-coupled transistors. The gain of the second stage (T3/T4) is preset by means of P1. The total gain should not be set higher than is necessary to ensure good reception, otherwise the receiver becomes oversensitive and prone to interference.

To prevent the circuit being triggered by spurious pulses, the amplifier is followed by a voltage comparator with an adjustable threshold (R13/R15/P2 and N1). The trigger threshold may be varied by means of P2, and the best setting for this potentiometer should be determined experimentally.

Once the signal has passed the trigger stage it is rectified, then buffered by N2 and N3, before being fed to the audio generator N4 (figure 2b).

2b



2c

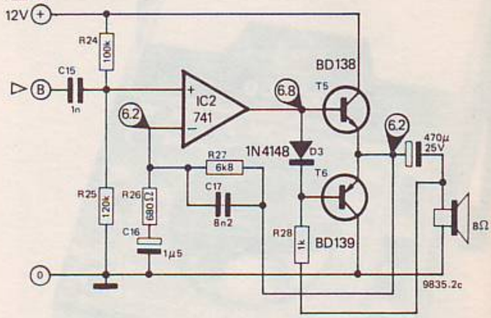


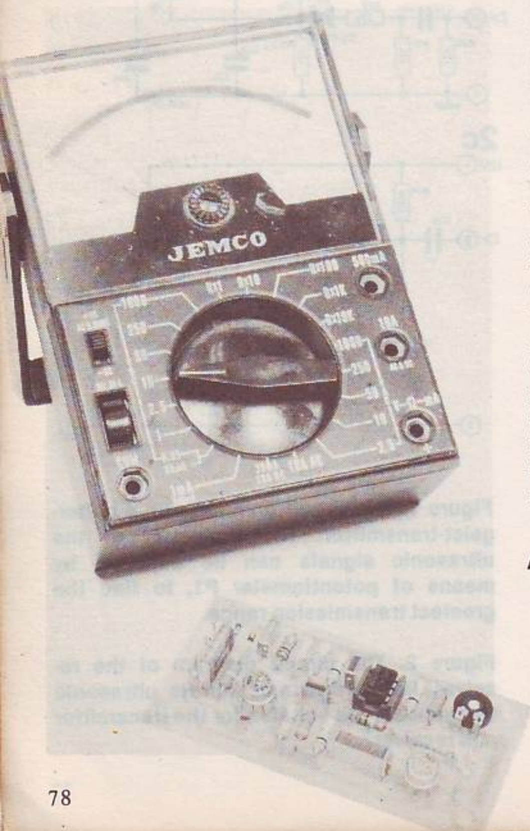
Figure 1. The circuit diagram of the poltergeist-transmitter. The frequency of the ultrasonic signals can be adjusted by means of potentiometer P1, to find the greatest transmission range.

Figure 2. The circuit diagram of the receiver. Both Valvo and Murata ultrasonic transducers are suitable for the transmitter and receiver.

This gate is connected as an inverter, and feedback is applied via a twin-T filter network. At the resonant frequency f_0 the phase shift of the twin-T network is 180°, so that the stage will oscillate at this frequency.
P3 should be adjusted so that the audio generator just fails to oscillate under quiescent conditions. Only when the oscillator receives a trigger pulse from N3 will it produce an output in the form of a decaying oscillation. With the component values shown, the resultant sound is similar to that of someone rapping their knuckles on a wooden table. The tone of this sound can be altered by varying the values of R18, R19, R23, C11, C12 and C13.
Finally, IC2, T5 and T6 form a very simple audio amplifier which drives an 8 Ω loudspeaker (figure 2c). The output power of 2-3 watts may appear a little modest, however the resulting sound will bear full comparison with anything even the most troublesome of poltergeists can muster.

63 Analogue frequency meter

A true 'universal meter' should be able to read not only voltage, current and resistance – but also other quantities. The usual multimeter will only do this when used as a 'mainframe' in conjunction with 'plug-ins', that convert the input quantity into a form suitable for feeding into the actual meter. This circuit is for a 'frequency plug-in' that will enable any multimeter (or voltmeter) to read frequencies between 10 Hz and 10 kHz.



To measure frequency one does not immediately have to 'go digital'. The analogue approach will invariably prove simpler and cheaper, in particular when the analogue readout (the multimeter) is already to hand. All that is needed is a plug-in device, a 'translator', that will give the meter an input it can 'understand'. This design is based upon an integrated frequency-to-voltage converter, the Raytheon 4151. The device is actually described as a voltage-to-frequency converter; but it becomes clear from the application notes that there is more to it than just that. The linearity of the converter IC is about 1%, so that a reasonably good multimeter will enable quite accurate frequency measurements to be made.
Because the 4151 is a little fussy about the waveform and amplitude of its input signal, the input stage of this design is a limiter-amplifier (comparator). This stage will process a signal of any shape, that has an amplitude of at least 50 mV, into a form suitable for feeding to the 4151. The input of this stage is protected (by diodes) against voltages up to 400 V p-p. The drive to the

A few specifications:

frequency range:	10 Hz...10 kHz
input impedance:	> 560 k
sensitivity:	50 mV p-p
max input voltage:	400 V peak
minimum load on output:	5 k (if 10 V out required)

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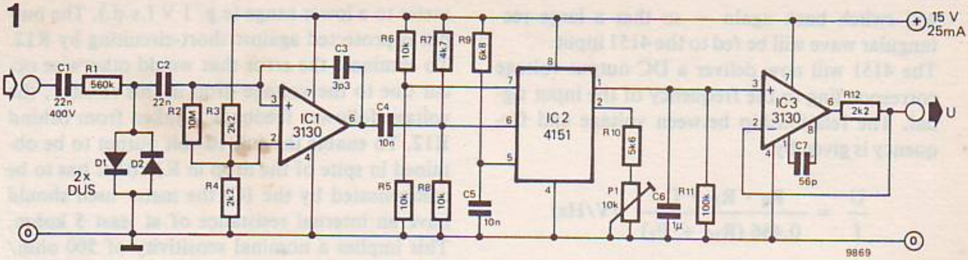


multimeter is provided by a short-circuit-proof unity-gain amplifier.

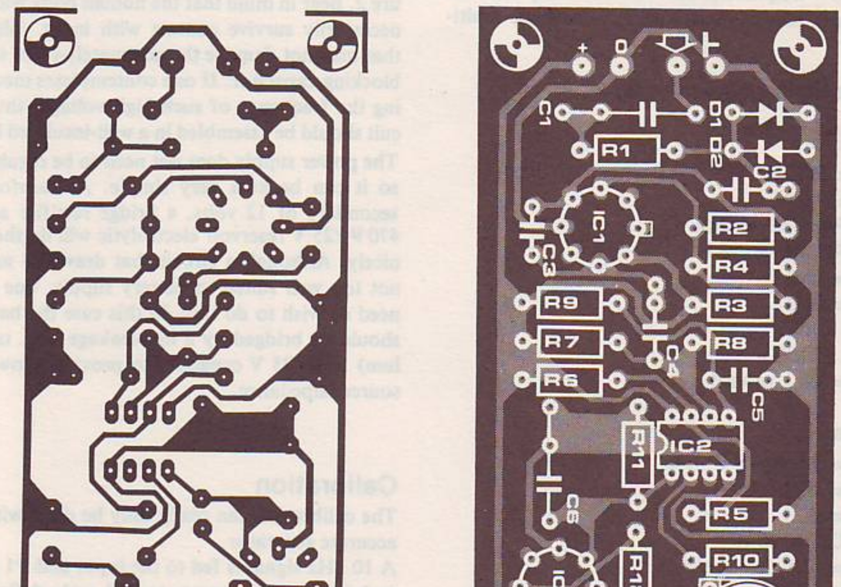
The circuit

Figure 1 gives the complete circuit of the frequency plug-in. The input is safe for 400 V p-p AC inputs only when the DC blocking capacitor is suitably rated. The diodes prevent excessive drive voltages from reaching the input of the comparator IC1. The inputs of this IC are biased to half the supply voltage by the divider R3/R4. The bias current flowing in R2 will cause the output of IC1 to saturate in the negative direction. An input signal of sufficient amplitude to overcome this offset will cause the output to change state, the actual switchover being speeded up by the positive feedback through C3. On the opposite excursion of the input signal the comparator

Figure 1. The input frequency is passed via a comparator (limiter) IC1 to a frequency-to-voltage converter (IC2, 4151), that delivers a DC voltage via buffer IC3 to a normal multimeter.

Figure 2. Printed circuit board and component layout for the frequency 'add-on'

2



will switch back again – so that a large rectangular wave will be fed to the 4151 input.

The 4151 will now deliver a DC output voltage corresponding to the frequency of the input signal. The relationship between voltage and frequency is given by:

$$\frac{U}{f} = \frac{R_9 \cdot R_{11} \cdot C_5}{0.486\,(R_{10} + P_1)} \text{ (V/Hz)}$$

The circuit values have been chosen to give 1 V per kHz. This means that a 10 volts f.s.d. will correspond to 10 kHz. Meters with a different full scale deflection, for example 6 volts, can, however, also be used. There are two possibilities: either one uses the existing scale calibrations to read off frequencies to 6 kHz, or one sets P1 to achieve a 6 volt output (i.e. full scale in our example) when the frequency is 10 kHz. The latter choise of course implies that every reading will require a little mental gymnastics! With some meters it may be necessary to modify the values of P1 and/or R10; the value of R10 + P1 must however always be greater than 500 Ω.

The output is buffered by another 3130 (IC3). The circuit is an accurate voltage follower, so that low frequencies can be more easily read off (without loss of accuracy) by setting the multimeter to a lower range (e.g. 1 V f.s.d.). The output is protected against short-circuiting by R12. To eliminate the error that would otherwise occur due to the voltage drop in this resistor, the voltage follower feedback is taken from behind R12. To enable the full 10 volt output to be obtained in spite of the drop in R12 (that has to be compensated by the IC) the meter used should have an internal resistance of at least 5 kohm. This implies a nominal sensitivity of 500 ohm/volt on the 10 volt range. There surely cannot be many meters with a sensitivity lower than that. If one has a separate moving coil milliameter available, it can be fitted with a series resistor that makes its internal resistance up to the value required of a voltmeter giving f.s.d. at 10 volt input. This alternative makes the frequency meter independent of the multimeter, so that it can be used to monitor the output of a generator that for some reason may have a dubious scale- or knob-calibration.

Parts list for figures 1 and 2.

Resistors:
R1 = 560 k
R2 = 10 M
R3, R4, R12 = 2k2
R5, R6, R8 = 10 k
R7 = 4k7
R9 = 6k8
R10 = 5k6
R11 = 100 k
P1 = 10 k preset

Capacitors:
C1 = 22 n/400 V
C2 = 22 n
C3 = 3p3
C4, C5 = 10 n
C6 = 1 µ low leakage
C7 = 56 p

Semiconductors:
D1, D2 = DUS
IC1, IC3 = 3130
IC2 = 4151

Construction

No trouble is to be anticipated if the circuit is built up using the PC board layout given in figure 2. Bear in mind that the human body will not necessarily survive contact with input voltages that may not damage the adequately-rated input blocking capacitor. If one contemplates measuring the frequency of such high voltages the circuit should be assembled in a well-insulated box!

The power supply does not need to be regulated, so it can be kept very simple. A transformer secondary of 12 volts, a bridge rectifier and a 470 µ /25 V reservoir electrolytic will do the job nicely. Although a circuit that draws 25 mA is not too well suited to battery supply, one may need or wish to do this. In this case the battery should be bridged by a low-leakage (e.g. tantalum) 10 µ /25 V capacitor to provide a low AC source impedance.

Calibration

The calibration can really only be done with an accurate generator.

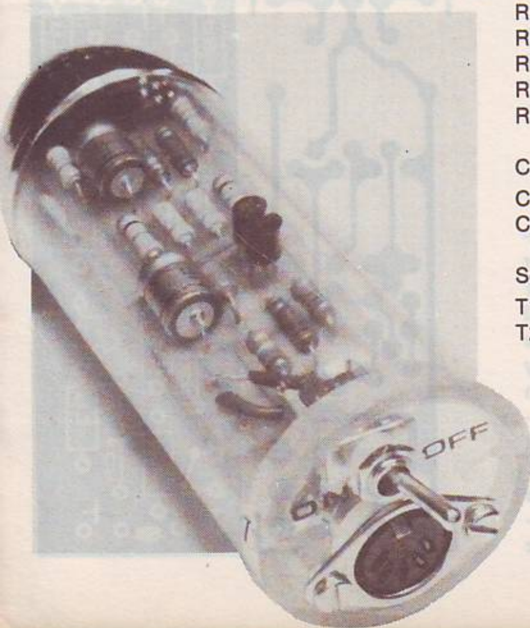
A 10 kHz signal is fed to the input and P1 is set to bring the multimeter to full scale deflection (e.g. 10 V). That completes the calibration – although it is wise to check that the circuit is operating correctly by using lower input frequencies and observing whether the meter reading is also (proportionately) lower.

64 Electret microphone preamplifier

This compact, low-noise, battery powered preamplifier can be used to boost the signal from electret and low impedance dynamic microphones.

Microphones frequently have to be connected to amplification and/or recording equipment via several metres of screened cable. Since the output of a microphone is very small (typically a few millivolts) there is often significant signal loss, and microphonic noise may also be generated by the cable. This article describes the construction of a good-quality microphone with built-in preamplifier, using a commercial electret or moving coil capsule. The built-in preamplifier boosts the output level to several hundred millivolts, which allows the signal to be fed direct to the 'auxiliary' or 'line' inputs of amplifiers or tape decks. If a mixer is being used the need for microphone preamps on each mixer input is dispensed with.
Readers are probably familiar with the principle of the moving coil, dynamic microphone, which basically operates like a loudspeaker in reverse. A diaphragm is coupled to a cylindrical coil, which is suspended in the field of a powerful permanent magnet. Sound pressure waves deflect the diaphragm, and hence the coil, which cuts the magnetic flux lines and generates an output current and voltage that is an electrical analogue of the acoustic signal.
The electret microphone, which has become very popular in recent years, operates in a similar manner to a capacitor microphone, but is cheaper and less bulky. The diaphragm of the microphone is made of the electret material. This is a thin insulating plastic film, which has been polarised with a permanent electric charge (this is usually done by heating the film and placing it in a strong electric field). The diaphragm forms one plate of a capacitor, the other plate of which is a fixed metal backplate. Since the diaphragm is charged a potential difference exists between the diaphragm and the backplate, which is related to the charge on the diaphragm and the capacitance of the microphone capsule by the equation

$$U = \frac{Q}{C},$$



Parts list for figures 1 and 2

Resistors:

R1 = 2k2
R2 = 10 k
R3 = 47 Ω
R4 = 6k8
R5, R6 = 39 k
R7 = 4k7
R8 = 8k2
R9 = 120 k

Capacitors:

C1, C2, C5 = 2 µ2/40 V
C3, C4 = 47 µ /25 V

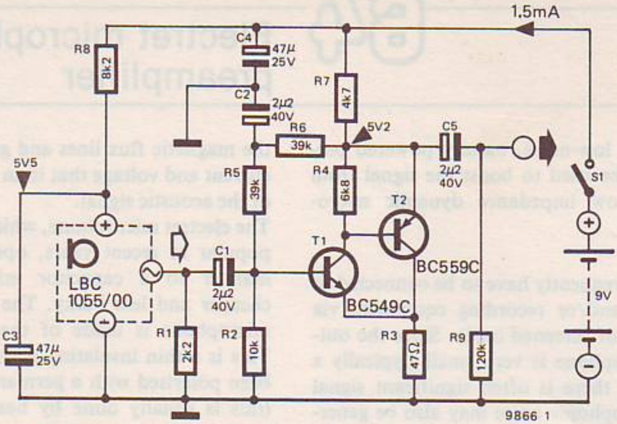
Semiconductors:

T1 = BC 549C or equivalent
T2 = BC 559C or equivalent

Miscellaneous:

Microphone capsule = Philips LBC 1055/00 or similar
9 V battery
S1 = SPST switch (see text)
Plastic or aluminium tubing for microphone housing.

1



where U is voltage, Q is charge, and C is capacitance. C is related to the distance between the plates of the capacitor by the equation

$$C = \frac{k}{d}$$

where k is a constant. Therefore

$$U = \frac{Qd}{k}.$$

When sound pressure waves deflect the diaphragm, the distance d varies, and since the charge Q is fixed the output voltage varies in sympathy with the deflection of the diaphragm. Since the microphone capsule is effectively a very small capacitor (only a few pF), its impedance at audio frequencies is extremely high, and its output must be fed to a very high impedance buffer stage. This usually consists of a FET source-follower incorporated into the microphone capsule, which acts as an impedance transformer with an output impedance of a few hundred ohms.

Preamplifier circuit

The complete circuit of the microphone preamplifier is given in figure 1. If an electret microphone capsule is used, the built-in FET buffer will require a DC power supply. This will usually be lower than the 9 volts required by the rest of the circuit, so the voltage is dropped by R8 and decoupled by C3. The value of R8 shown is for the Philips LBC 1055/00 microphone capsule, and other capsules may require a different value.

Resistor R1 is a load for the FET buffer. Here again, 2k2 is the recommended value for the Philips electret capsule, and different values may be

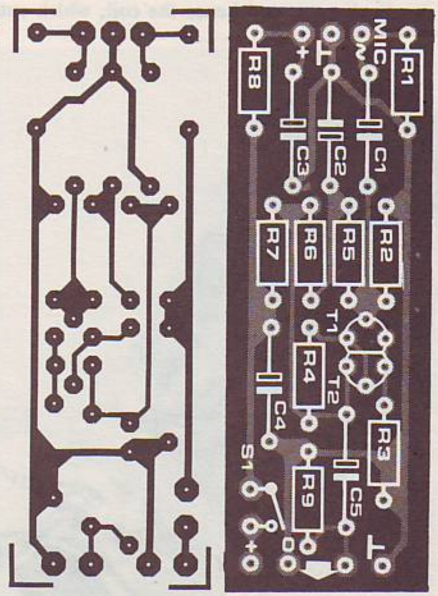
Figure 1. Circuit of the microphone preamplifier.

Figure 2. Printed circuit board and component layout for the preamplifier (EPS 9866).

Figure 3. If the completed microphone is fitted with an output socket then a shorting link can be used to replace S1.

Photo. Completed prototype of the electret microphone with built-in preamp, which is housed in a piece of clear acrylic tube for display purposes.

2

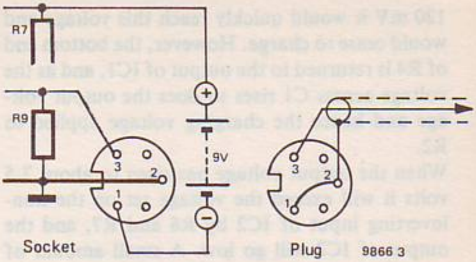


required for other capsules. If a moving coil microphone capsule is used then R1, R8 and C3 may be omitted.
The preamplifier itself consists of a two stage amplifier T1 and T2. Its input impedance is approximately 8 k, and its gain is determined by the ratio R7 : R3 – about 100 with the values shown. The current consumption of the preamp is extremely low, typically 1.5 mA.
With some microphone capsules having a higher output voltage, it may be necessary to reduce the gain of the preamp to prevent overloading. This is done by decreasing the value of R7. To restore the correct DC bias conditions it will also be necessary to reduce the value of R6, and this will result in a slight increase in current consumption. However, reducing the value of R7 does lower the output impedance of the preamp, which means that longer cables can be driven without attenuation of high frequency signals.

Performance

The output voltage of the specified electret capsule is typically 6.3 mV/Pa ('Pa' is Pascal; 1 Pascal = 1 N/m² = 10 bar). To put this figure into context, the threshold of audibility (0 dB SPL) is taken as occurring at a sound pressure level of 0.0002 bar, and the threshold of pain, 120 dB higher at 200 bar. However, overloading of the electret capsule begins at around 104 dB SPL, so the maximum output voltage that can be expected in normal use is around 20 mV, or 2 V at the preamp output.
The frequency response of the specified capsule

3



plus preamp combination is flat within 3 dB from 100 Hz to 17 kHz, which is quite good considering the modest cost of the unit.

Construction

A printed circuit board and component layout for the microphone preamplifier are given in figure 2. The circuit board is extremely compact, and the microphone capsule, board, and a small 9 V battery can easily be fitted into a length of plastic pipe or aluminium tubing. The grille that protects the microphone capsule can be made from half a 'tea-egg' infuser, as shown in the photograph, or from a wire mesh coffee strainer.
To make a really professional job the output of the preamp can be taken via a Cannon XLR or locking DIN connector socket mounted in the base of the housing. It is then possible to dispense with the on-off switch by making a shorting link in the connector plug, as shown in figure 3. When the microphone is unplugged after use the preamp is automatically switched off.

65 Long interval timer

The drawback of most analogue timers (monostable circuits) is that, in order to obtain reasonably long intervals, the RC time constant must be correspondingly large. This invariably means resistor values in excess of 1 MΩ, which can give timing errors due to stray leakage resistance in the circuit, or large electrolytic capacitors, which again can introduce timing errors due to their leakage resistance.
The circuit given here achieves timing intervals up to 100 times longer than those obtainable with standard circuits. It does this by reducing the charging current of the capacitor by a factor of 100, thus increasing the charging time, without the need for high value charging resistors.
The circuit operates as follows: when the start/reset button is pressed C1 is discharged and the output of IC1, which is connected as a voltage follower, is at zero volts. The inverting input of comparator IC2 is at a lower potential than the non-inverting input, so the output of IC2 goes high.
The voltage across R4 is approximately 120 mV, so C1 charges through R2 at a current of around 120 nA, which is 100 times lower than could be achieved if R2 were connected direct to positive supply.
Of course, if C1 were charged from a constant

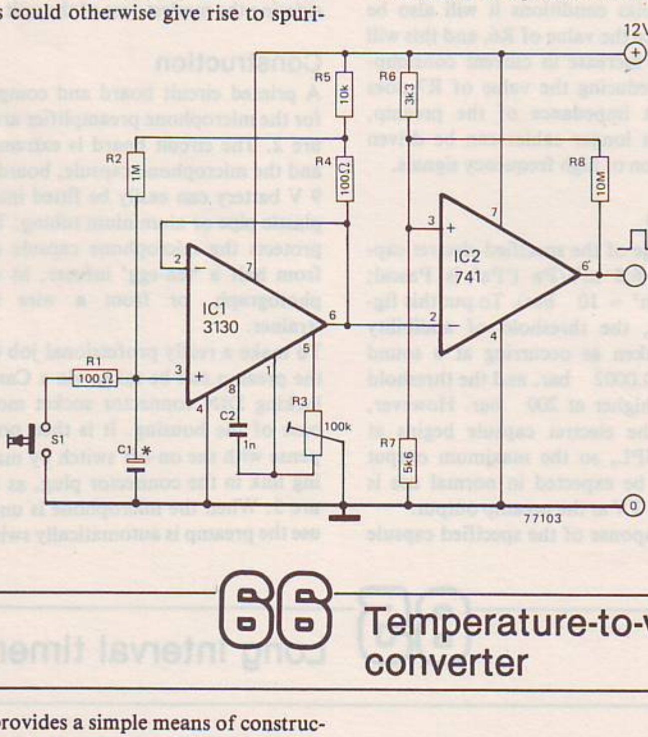
120 mV it would quickly reach this voltage and would cease to charge. However, the bottom end of R4 is returned to the output of IC1, and as the voltage across C1 rises so does the output voltage and hence the charging voltage applied to R2.

When the output voltage has risen to about 7.5 volts it will exceed the voltage set on the non-inverting input of IC2 by R6 and R7, and the output of IC2 will go low. A small amount of positive feedback provided by R8 prevents any noise present on the output of IC1 from being amplified by IC2 as it passes through the trigger point, as this could otherwise give rise to spurious output pulses.

The timing interval is given by the equation:

$$T = R_2C_1 \left(1 + \frac{R_5}{R_4} + \frac{R_5}{R_2}\right) \ln \left(1 + \frac{R_7}{R_6}\right)$$

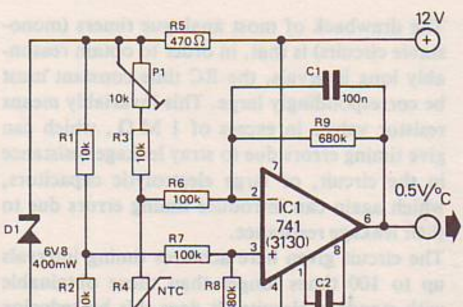
This may seem a little complicated, but with the component values given the interval is 100 · C1, where C1 is in *microfarads*, e.g. if C1 is 1 μ the interval is 100 seconds. It is evident from the equation that the timing interval can be varied linearly by replacing R2 with a 1 M potentiometer, or logarithmically by replacing R6 and R7 with, say, a 10 k potentiometer.



66 Temperature-to-voltage converter

This circuit provides a simple means of constructing an electronic thermometer that will operate over the range 0 to 24°C (32 to 75°F). The circuit produces an output of approximately 500 mV/°C, which can be read off on a voltmeter suitably calibrated in degrees.

In order that the circuit should be kept simple the temperature sensing element is a negative temperature coefficient thermistor (NTC). This has the advantage that the temperature coefficient of resistance is fairly large, but unfortunately it has the disadvantage that the temperature coefficient is not constant and the temperature-voltage output of the circuit is thus non-linear. However, over the range 0 to 24°C the

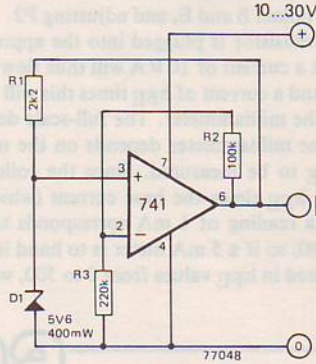


linearity is sufficiently good for a simple thermometer.
Op-amp IC1 is connected as a differential amplifier whose inputs are fed from a bridge circuit consisting of R1 to R4. R1, R2, R3 and P1 form the fixed arms of the bridge, while R4 forms the variable arm. The voltage at the junction of R1 and R2 is about 3.4 volts. With the NTC at 0°C P1 is adjusted so that the output from the op-amp is zero, when the voltage at the junction of R3 and R4 will also be 3.4 V. With increasing temperature the resistance of the NTC decreases and the voltage across it falls, so the output of the op-amp increases. If the output is not exactly 0.5 V/°C then the values of R8 and R9 may be increased or decreased accordingly, but they should both be the same value.
The IC can be a general purpose op-amp such as a 741, 3130 or 3140. The compensation capacitor C2 is not required if a 741 is used since this IC is internally compensated. Almost any 10 k NTC thermistor may be used for R4, but the smaller types will obviously give a faster response since they have a lower thermal inertia. 5 k or 15 k types could also be used, but the values of P1 and R3 would have to be altered in proportion.

67 Super zener

This circuit is intended primarily to produce a stable reference voltage in battery operated equipment designed for minimum current consumption. Despite the fact that only 1 mA flows through the zener the output voltage showed a fluctuation of less than 1 mV for supply voltage variations of 10 to 30 volts.
The reference voltage from the zener is applied to the non-inverting input of a 741 op-amp, and the output voltage is the zener voltage multiplied by the op-amp gain i.e.

$$V_O = V_Z \times \frac{R_2 + R_3}{R_3}$$



This approach has two advantages. Firstly, a low temperature coefficient zener (5.6 V) can be used to provide any desired reference voltage simply by altering the op-amp gain. Secondly, since no significant current is 'robbed' from the zener by the op-amp input, the zener need only be fed by a small current. So that the resistance of the zener does not affect the output voltage the zener current must be fairly constant. This is achieved by feeding the zener via R1 from the output of the op-amp. The zener current is

$$\frac{V_O - V_Z}{R_1},$$

so R1 should be chosen to give a zener current of about 1 mA. The reference voltage obtained from the op-amp output can supply currents of up to 15 mA.
One point to note when using this circuit is that the supply voltage must be at least 2 V greater than the output voltage of the circuit.

68 Simple transistor tester

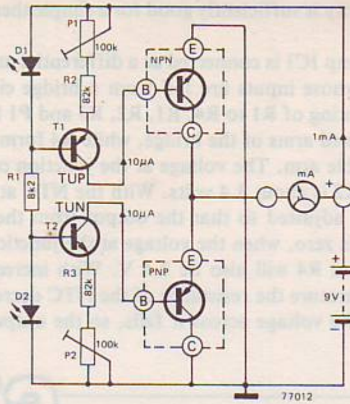
This simple circuit checks the functioning and measures the current gain (h_{FE}) of PNP or NPN bipolar transistors. It operates by feeding a known constant current into the base of the transistor and measuring the collector current. Since the collector current of a non-saturated

transistor is h_{FE} times the base current (which is known) it is a simple matter to calculate the value of h_{FE}, and in fact the meter which measures the collector current can be calibrated directly in h_{FE}.

Since both PNP and NPN transistors must be tested, two constant current sources are required, to provide a negative base current for PNP transistors and a positive base current for NPN transistors. The voltage dropped across the LED causes a constant current to flow through the emitter resistor of the TUP and a corresponding constant collector current, which flows into the base of the NPN transistor under test. This current can be set to 10 μA by connecting a 50 μA meter between points B and E and adjusting P1.

The lower LED and TUN constitute the negative current source. Here again, this may be set to 10 μA by connecting a microammeter between the lower points B and E, and adjusting P2.

When a transistor is plugged into the appropriate socket a current of 10 μA will thus flow into the base and a current of h_{FE} times this will flow through the milliammeter. The full-scale deflection of the milliammeter depends on the maximum h_{FE} to be measured. Since the collector current is h_{FE} times the base current (which is .01 mA) a reading of 1 mA corresponds to an h_{FE} of 100, so if a 5 mA meter is to hand it can be calibrated in h_{FE} values from 0 to 500, which



should be adequate for most run-of-the-mill transistors. However, for testing 'C' versions of small-signal transistors, which can have gains up to 800, a 10 mA meter calibrated 0 to 1000 could be used, or lower f.s.d. meter shunted to read 8 mA and calibrated 0 to 800.

Readers may have noticed that it is actually the emitter current of the PNP transistor that is measured, which is of course $1 + h_{FE}$ times the base current. However, since few transistors have gains less than 50 the worst error introduced by this is less than 2%, which is probably less than the error of the milliammeter.

69 Automatic NiCad charger

It is not generally appreciated that, if Nickel-Cadmium batteries are subjected to prolonged overcharging from chargers of the constant current type, their life may be considerably reduced.

The charger described here overcomes this problem by charging at a constant current but switching off the charger when the terminal voltage of the battery rises, which indicates a fully-charged

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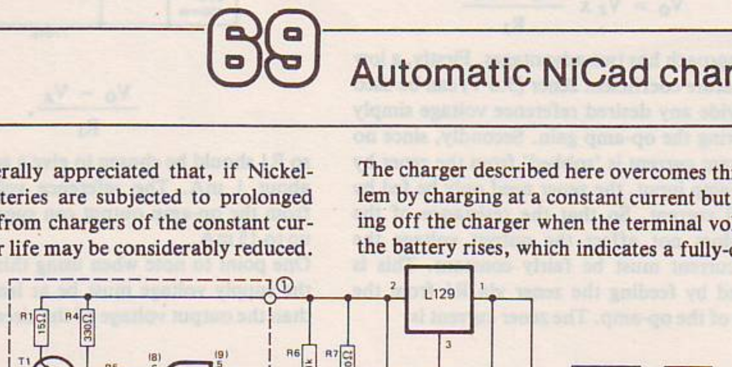

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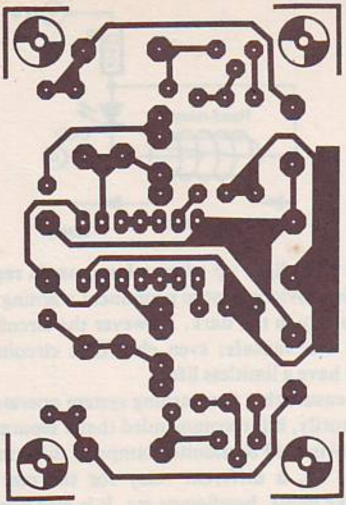
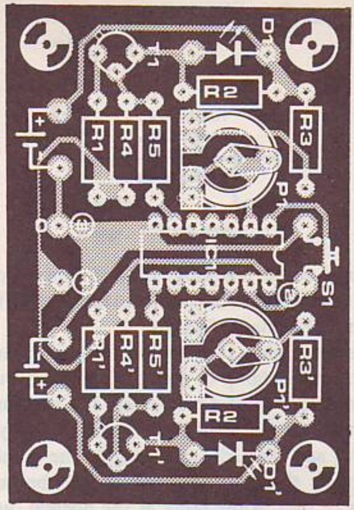




condition. The basic circuit described is intended to charge a single 500 mAh 'AA' cell at the recommended charge rate of around 50 mA, but it can easily be extended at little cost to charge more than one cell.

Power for the circuit is provided by a transformer, bridge rectifier and 5 V IC regulator. The cell is charged by a constant current source T1 which is controlled by a voltage comparator based on a TTL Schmitt trigger N1. While the cell is charging the terminal voltage remains at around 1.25 V, which is below the positive trigger threshold of N1. The output of N1 is thus high, the output of N2 is low and T1 receives a base bias voltage from the potential divider R4/R5. While the cell is being charged D1 is lit.

When the cell approaches the fully-charged state the terminal voltage rises to about 1.45 V, the positive trigger threshold of N1 is exceeded and the output of N2 goes high, turning off T1. The cell ceases to charge and D1 is extinguished.

As the positive trigger threshold of N1 is about 1.7 V and is subject to a certain tolerance, R3 and P1 are included to adjust it to 1.45 V. The negative trigger threshold of the Schmitt trigger is about 0.9 V, which is below the terminal voltage of even a fully-discharged cell, so connecting a discharged cell in circuit will not cause charging to begin automatically. For this reason a start button S1 is included which, when pressed, takes the input of N1 low.

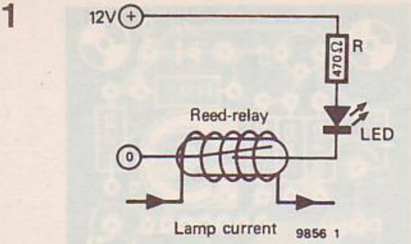
To charge a number of cells the portion of the circuit enclosed in the dotted box must be duplicated. This has the advantage that, unlike chargers in which cells are connected in series, cells in any state of discharge may be placed on the charger and each will be individually charged to the correct level. The disadvantage is that batteries of cells cannot be charged. However, up to ten AA cells may be charged if the circuit is duplicated the appropriate number of times.

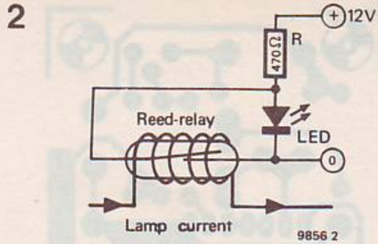
H. Knote

70 Car lights failure indicator

It is often the case that the first a motorist knows of a failure in one of his car lights is when his attention is drawn to the fact by a policeman. The circuit described here, which consists solely of a single reed-relay, one LED and one resistor, should provide a more economical warning system.

A LED is mounted in a suitable spot on the dashboard, and is extinguished as soon the lamp





concerned ceases working. It is of course possible to use several such circuits to monitor different lamps or groups of lamps.

The circuit (figure 1) works by feeding the supply current to a lamp or group of lamps through the operating coil of a reed-relay. If a particular lamp fails, the current falls, causing the relay to drop out and the LED to turn off. The number of turns in the operating coil should be large enough to pull in the relay at the normal operating current of the lamp, yet small enough to cause the relay to drop out in the event of lamp failure.

Generally speaking, a relay requires from 30 to 100 AT (ampere turns = current x no. of turns). Thus, in view of the relatively high currents drawn by car lamps, in this particular application the operating coil need consist of only a few turns. For example, the two headlamps draw a current of approx. 7.5 A (at 12 V). A reed-relay rated at 50 AT would therefore require only 7 turns to monitor the current of both headlamps. If one of the lamps fails, then the current through the operating coil falls to about half, causing the relay to drop out and the LED on the dashboard to be extinguished. The circuit shown in figure 2 is an alternative version which makes the LED light up when a lamp needs replacing. This provides a more prominent warning – particularly in the dark. However the circuit in figure 1 is failsafe; even electronic circuitry does not have a limitless life...

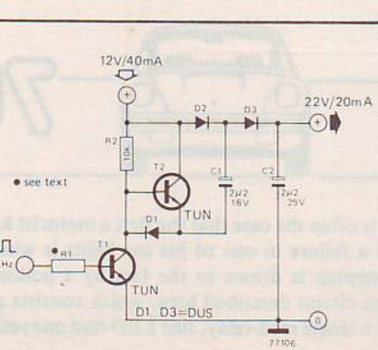
To ensure that the warning system operates satisfactorily, it is recommended that a separate reed-relay is used to monitor lamps of differing wattage, i.e. a different relay for the rear lights, brake lights, headlamps etc. It is also possible to use a single relay to monitor both right and left turning indicators by using a double winding round the coil. However, it is not advised to use one relay to monitor a circuit or combination of circuits in which more than two lamps can be 'on' simultaneously.

If the circuit of figure 2 is used then the supply to the LED should be taken from the switched side of the lamp supply. This ensures that when the relay drops out due to the lamp being switched off the LED does not light, since its supply is also disconnected.

It is important to note that the gauge of wire used to wind the relay coil should be at least as heavy as that used in the original car wiring, to minimise the voltage drop across the coil and possible overheating.

71 Two-TUN voltage doubler

This little circuit will produce a DC output that is almost twice the supply voltage. A square-wave input is required of sufficient level to turn T1 fully on and off. When T1 is conducting, C2 is charged to just under the supply voltage. When T1 is cut off, T2 starts to conduct and raises the voltage at the negative end of C2 to just under the positive supply level. This implies that the voltage at the positive end of C2 is raised to almost twice the supply voltage, so that C3 will ultimately charge to this level.



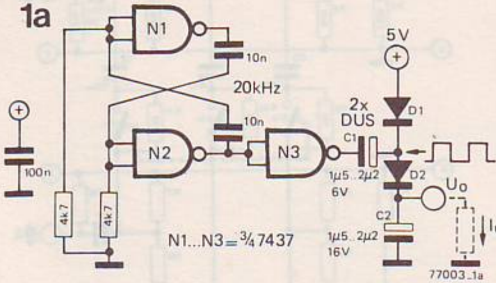
The circuit is remarkably efficient: the current drawn from the main supply is only marginally greater than twice the output current. In the example shown here, the efficiency is approximately 90%.

The value for R1 depends on the amplitude of the square-wave input: T1 will require a base current of 0.5...1 mA.

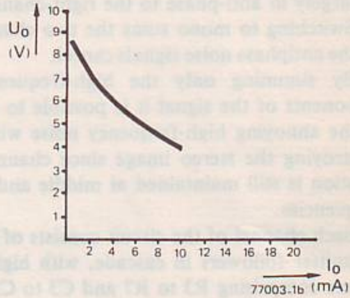
RCA application note

72 TTL voltage doubler

1a



1b

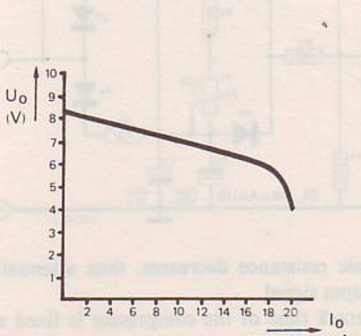


This voltage doubler can be used in circuits that have only a 5 V supply rail, where a higher voltage is required at a low current.

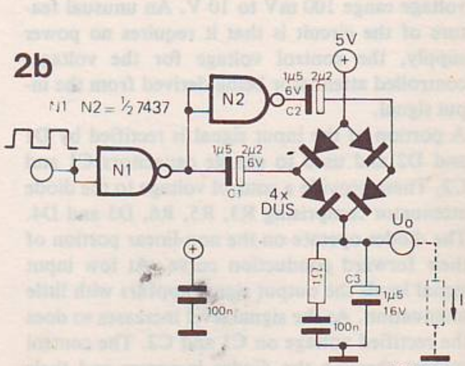
Figure 1a shows the basic circuit, which uses three of the gates in a 7437 quad two-input NAND buffer IC. N1 and N2 are connected as a 20 kHz astable multivibrator, and the output of N2 drives N3, which acts as a buffer between the astable and the doubler circuit. When the output of N3 is low C1 charges through D1 and N3 to about +4.4 V. When the output of N3 goes high the voltage on the positive end of C1 is about 9 V, so C1 discharges through D2 into C2. If no current is drawn from C2 it will eventually charge to about +8.5 V. However, if any significant current is drawn the output voltage will quickly fall, as shown in figure 1b.

Much better regulation of the output voltage, as shown in figure 2a, can be obtained by using the push-pull circuit of figure 2b. This is driven from an identical astable to that in figure 1b. While the output of N1 is low and C1 is charging, the output of N2 is high and C2 is discharging into C3, and vice versa. Since C3 is being continually charged the regulation of the output voltage is much improved.

2a



2b



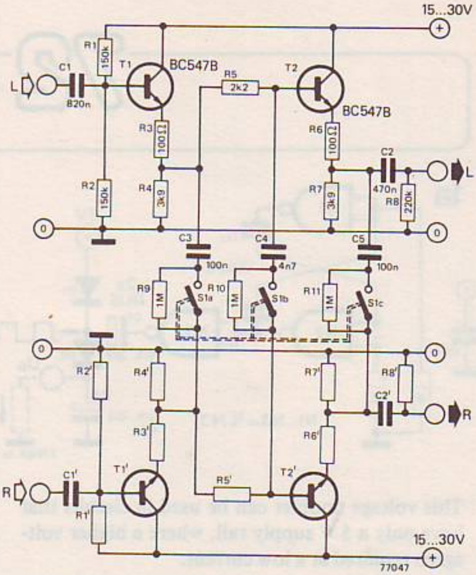
73 Stereo noise filter

The signal-to-noise ratio of an FM broadcast received in stereo is considerably worse than that of the same broadcast received in mono. This is most noticeable on weak transmissions, when switching over from stereo to mono will considerably reduce the noise level. This noise reduction occurs because the left-channel noise is largely in anti-phase to the right-channel noise. Switching to mono sums the two channels and the antiphase noise signals cancel.

By summing only the high-frequency components of the signal it is possible to eliminate the annoying high-frequency noise without destroying the stereo image since channel separation is still maintained at middle and low frequencies.

Each channel of the circuit consists of a pair of emitter followers in cascade, with highpass filters comprising R3 to R7 and C3 to C5 that allow crosstalk to occur between the two channels above about 8 kHz when switch S1 is closed. When S1 is open the two channels are isolated, but resistors R9 to R11 maintain a DC level on C3 to C5 so that switching clicks do not occur when S1 is closed.

The stereo-mono crossover frequency can be increased by lowering the values of C3 to C5 or decreased by raising them.



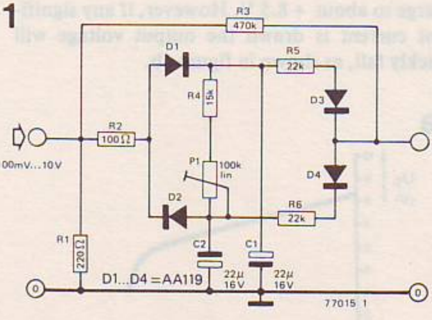
74 Signal powered dynamic compressor

This dynamic range compressor will provide approximately 20 dB of compression over the input voltage range 100 mV to 10 V. An unusual feature of the circuit is that it requires no power supply, the control voltage for the voltage-controlled attenuator being derived from the input signal.

A portion of the input signal is rectified by D1 and D2 and used to charge capacitors C1 and C2. These provide a control voltage to the diode attenuator comprising R3, R5, R6, D3 and D4. The diodes operate on the non-linear portion of their forward conduction curve. At low input signal levels the output signal appears with little attenuation. As the signal level increases so does the rectified voltage on C1 and C2. The control current through the diodes increases and their dynamic resistance decreases, thus attenuating the output signal.

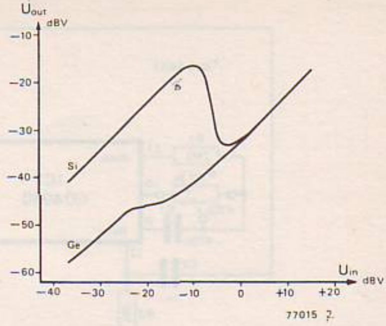
The attack time of the compressor is fixed and depends on the time constant consisting of C1 or

1



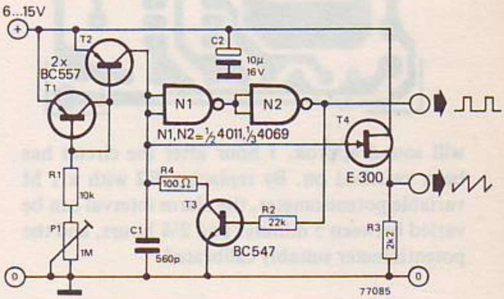
C2, R2 and the output impedance of the circuit feeding the compressor, which should be as low as possible. The decay time of the compressor can be varied to a small extent by P1. The input impedance of the circuit that the compressor output feeds should be as high as possible.
The circuit works best with germanium diodes, since these have a low forward voltage threshold and a much smoother and more extended 'knee' than silicon types. The accompanying graph shows the response of the compressor using both silicon and germanium diodes, and it is obvious which are better!

2



75 Sawtooth-CCO

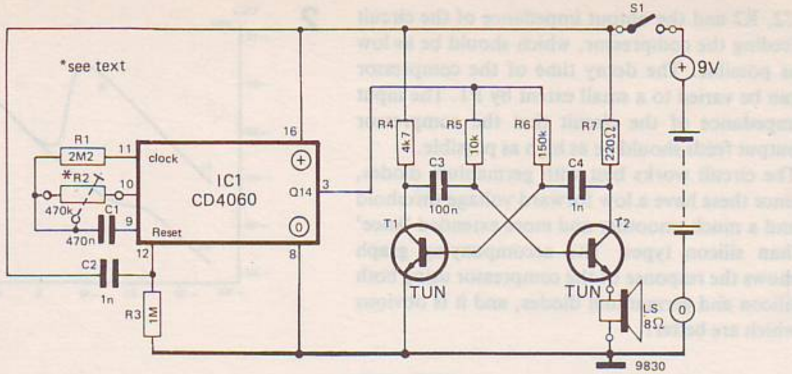
This sawtooth waveform generator which is built round a current controlled oscillator is distinguished by its large sweep range. It is suitable for use in electronic music applications, and the narrow output pulse also enables the circuit to be used as a pulse-CCO for sample/hold circuits.
The circuit consists of a controllable current source (T1, T2), a trigger (N1, N2) and a switch (T3). As soon as the circuit is switched on capacitor C1 is charged by the current source. When the voltage across C1 reaches the threshold value of N1, T3 is turned on via N1 and N2, and C1 is discharged, after which the whole cycle repeats itself. The sawtooth output signal which is buffered by FET T4 has a peak-to-peak value of approx. 1.3 V.
With the component values shown in the diagram, the frequency can be adjusted from approx. 5 to 500 kHz (with P1). Although a higher output frequency is possible, there is a corresponding deterioration in the waveform. With C1 = 5n6 and R1 = 1 k, the frequency range runs from 0.5…500 kHz.
In place of NANDs inverters may be used.



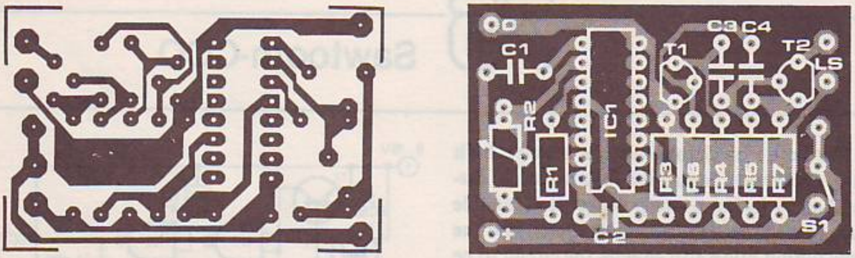
76 Knotted handkerchief

Since the advent of paper handkerchiefs, that time-honoured method of jogging a forgetful memory, namely tying a knot in one's hanky, has been faced with practical difficulties. The circuit described here offers a modern answer to this old problem, i.e. an electronic 'knot' in the shape of an audible alarm signal which can be set to sound after an interval of up to 60 minutes.
The circuit is built round the CMOS IC CD 4060, which consists of a pulse generator and a counter. When switch S1 is closed a reset pulse is fed to the IC via C2. At the same time the internal oscillator begins feeding pulses to the counter. After 2^{13} pulses the counter output (Q14) will go high, switching on the oscillator round T1 and T2. The result is a piercing 3 kHz signal which is made audible via an 8 ohm miniature loudspeaker or earpiece insert. The circuit is switched off by opening S1.
With the values given for R2 and C1, the 'knot'

1



2



will sound approx. 1 hour after the circuit has been switched on. By replacing R2 with a 1 M variable potentiometer, the alarm interval can be varied between 5 minutes and 2¼ hours, and the potentiometer suitably calibrated.

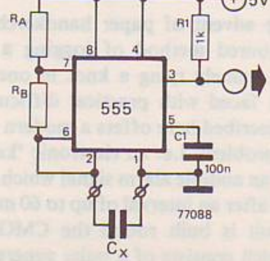
The circuit consumes very little current (0.2 mA whilst the counter is running and 35 mA during the alarm signal) so that a 9 V battery would be assured of a long life.

77 Digital capacitance meter with 555 timer

Anyone possessing a frequency counter with a facility for period measurement can build this simple add-on unit to measure capacitance direct.

In the circuit shown the 555 is connected as an astable multivibrator, the period of which is given by $T = 0.7(R_A + 2R_B)C_X$. If the unknown capacitor is connected in the C_X position then, since R_A and R_B are fixed, the period is proportional to C_X, the unknown capacitor. The period of the multivibrator can be measured by the period meter and, if R_A and R_B are suitably chosen, this reading can be made to equal the capacitance in picofarads, nanofarads or microfarads. As an example, suppose the period meter has a maximum reading of one second and this is to be the reading for a capacitance of 1 µ F. Then the total value of $R_A + 2R_B$ should be 1.43 MΩ .

A slight problem exists when measuring electrolytic capacitors around the 1 µ F value. As shown above, for a reading of one second the resistance required is fairly high and errors may occur due to the capacitor leakage resistance. In



this case it is probably better to opt for a reading of 1 second = 1000 µF, since the resistance values can be 1000 times smaller. If a seven decade counter is used that gives a reading of 1.000000 for one second = 1000 µF, then 1 µF will give a reading of 0.001000, which is still better than the accuracy of the circuit.

Some suitable values for R_A and R_B are given in the table. 1% metal oxide resistors should be used for these to give a reasonable accuracy. Other values can be calculated to suit personal taste and the counter used.

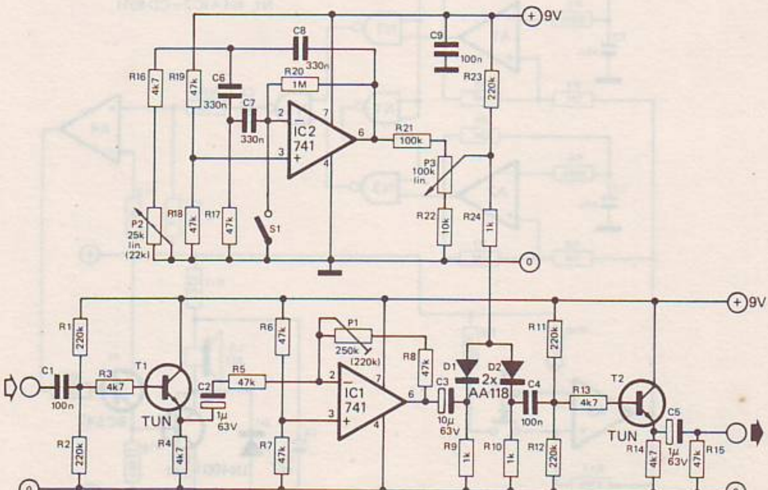
When using the circuit the wiring capacitance of any jigs and fixtures used to hold the capacitor should be taken into account and subtracted from the reading. For this reason, such jigs should be of rigid mechanical construction so that the capacitance does not vary. For example, in the prototype it was found that the circuit was reading consistently 36 pF high due to wiring capacitance. This was therefore noted on the test jig so that it could be subtracted from all readings. Of course, when testing large value capacitors this small error is not significant.

R_A	R_B	C_x	T
1 k	220 Ω	1000 µF	1 s
1 M	220 k	1 µF (non-electrolytic)	1 s

J. Borgman

78 Tremolo

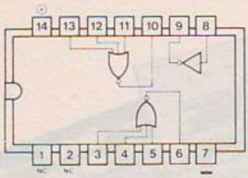
Tremolo is one of the most popular effects used in electronic music. The tremolo effect is produced by amplitude modulating the music signal with a low-frequency signal of between 1 Hz and 10 Hz. The effect gives warmth and richness to the otherwise 'flat' sound of instruments such as electronic organs. The most pleasing effect is produced when the modulation waveform is sinusoidal. The music signal is buffered by emitterfollower T1 and is then fed into op-amp IC1, whose gain can be varied by means of P1. The output of IC1 is fed to the diode modulator D1/D2, the output of which is buffered by a second emitter follower T2. The sinusoidal signal is generated by an oscillator built around IC2, whose frequency can be varied between 1 Hz and 10 Hz by P2. The output level, and hence the modulation depth, can be varied by P3. Switch S1, when closed, disables the oscillator, which allows the music signal to pass unmodulated.



BLANK

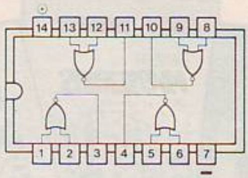
DUAL 3 INPUT NOR GATE PLUS INVERTER

4000



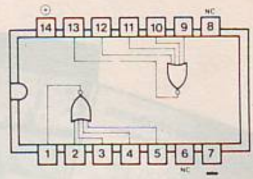
QUADRUPLE 2 INPUT NOR GATE

4001



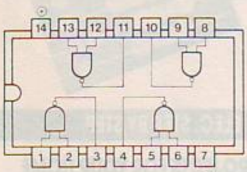
DUAL 4 INPUT NOR GATE

4002



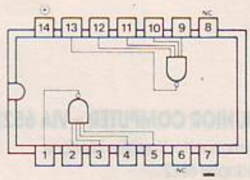
QUADRUPLE 2 INPUT NAND GATE

4011



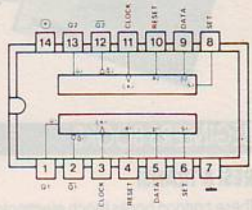
DUAL 4 INPUT NAND GATE

4012



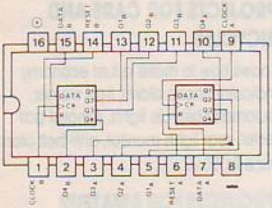
DUAL D FLIP FLOP

4013



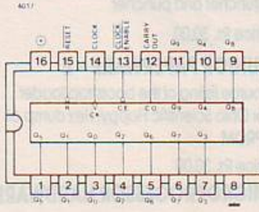
DUAL 4 BIT STATIC SHIFT REGISTER

4015



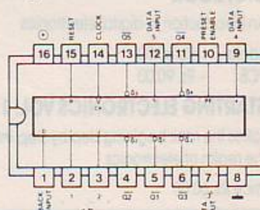
DIVIDE BY 10 SYNCHRONOUS COUNTER

4017



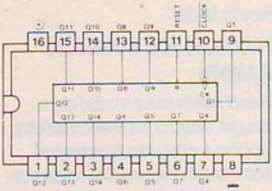
SYNCHRONOUS PRESETTABLE DIVIDE BY 'N' COUNTER

4018



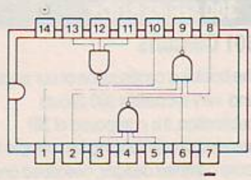
14 BIT BINARY RIPPLE COUNTER

4020



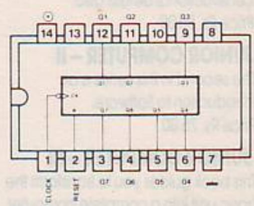
TRIPLE 3 INPUT NAND GATE

4023



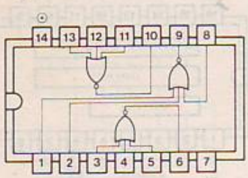
7 STAGE BINARY RIPPLE COUNTER

4024



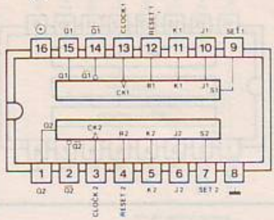
TRIPLE 3 INPUT NOR GATE

4025



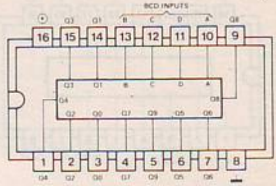
DUAL JK FLIP FLOP

4027



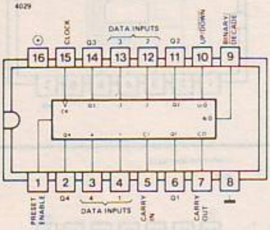
BCD TO DECIMAL DECODER

4028



SYNCHRONOUS PRESET TABLE BINARY/DECADE UP/DOWN COUNTER

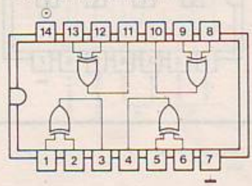
4029



QUADRUPLE 2 INPUT EXCLUSIVE OR GATES

4030

4070 low power TTL compatible (fan out - 2)

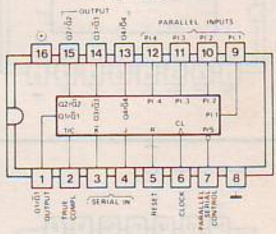


4035

4 BIT

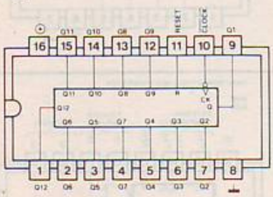
PARALLEL IN/PARALLEL OUT

SHIFT REGISTER



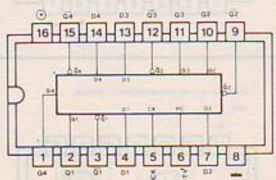
12 BIT BINARY RIPPLE COUNTER

4040



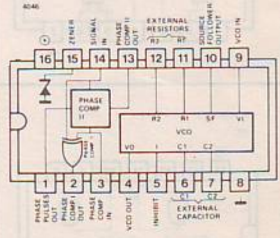
QUAD CLOCKED "D" LATCH

4042



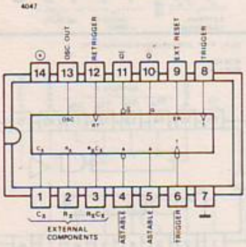
MICROPOWER PLL

4046



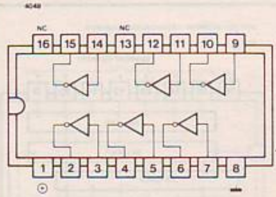
MONOSTABLE/ASTABLE MULTIVIBRATOR

4047



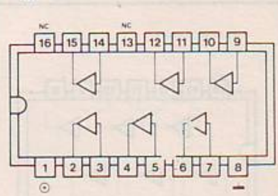
HEX INVERTING BUFFER

4049



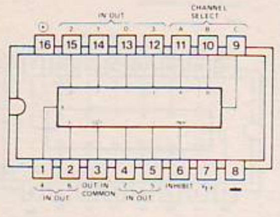
HEX BUFFER

4050



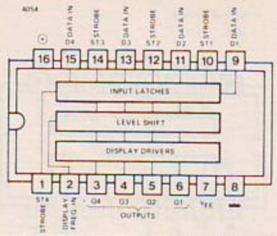
8 CHANNEL ANALOGUE MULTIPLEXER DEMULTIPLEXER

4051



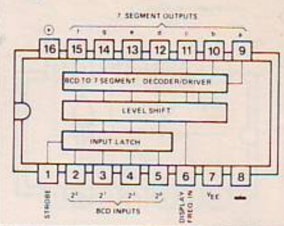
LCD DRIVER

4054



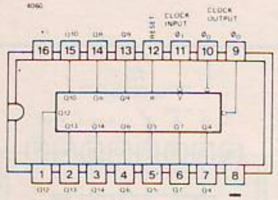
BCD TO 7 SEGMENT DECODER/DRIVER

4056



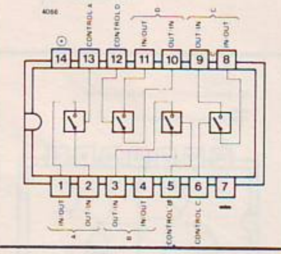
14 BIT BINARY RIPPLE COUNTER AND OSCILLATOR

4060



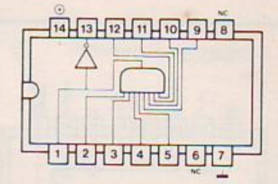
QUAD BILATERAL SWITCH

4066



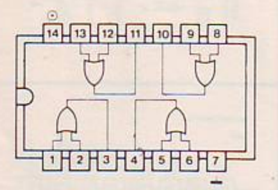
8 INPUT AND/NAND GATE

4068



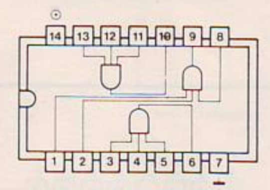
QUADRUPLE 2 INPUT OR GATE

4071



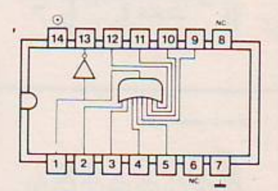
TRIPLE 3 INPUT AND GATE

4073



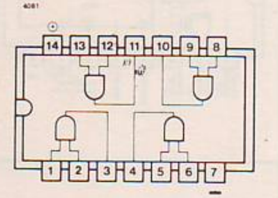
8 INPUT OR/NOR GATE

4078



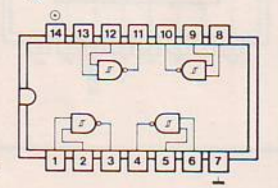
QUADRUPLE 2 INPUT AND GATE

4081



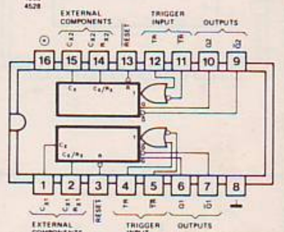
QUADRUPLE 2 INPUT NAND SCHMITT TRIGGER

4093



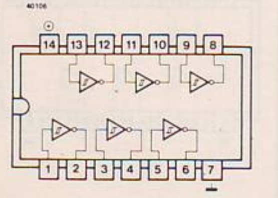
DUAL MONOSTABLE MULTIVIBRATOR

4098
4528



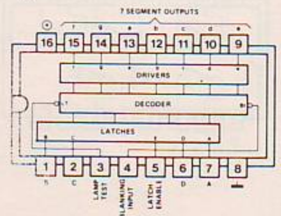
HEX SCHMITT TRIGGER

40106



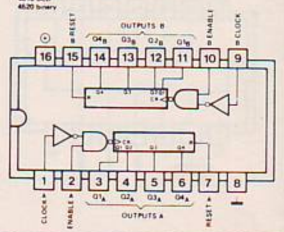
BCD TO 7 SEGMENT LATCH/DECODER/DRIVER

4511



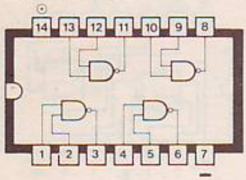
DUAL 4 BIT SYNCHRONOUS UP COUNTERS

4518 BCD
4520 binary



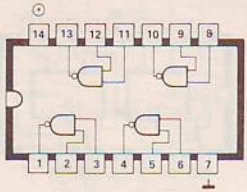
QUADRUPLE 2 INPUT NAND GATES

7400
7403 open collector outputs
7437 power driver (fan out = 30)



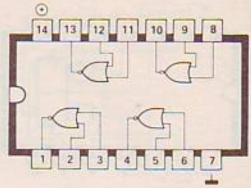
QUADRUPLE 2 INPUT NAND GATE WITH OPEN COLLECTOR OUTPUT

7401



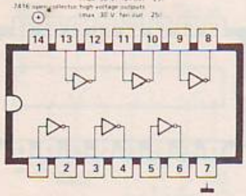
QUADRUPLE 2 INPUT NOR GATES

7402
7428 power driver (fan out = 30)



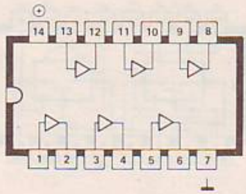
HEX INVERTERS

7404
7405 open collector outputs
7406 open collector high voltage outputs (max. 30 V; fan out = 25)
7416 open collector high voltage outputs (max. 30 V; fan out = 25)



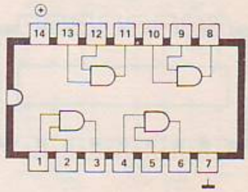
HEX BUFFER/DRIVER WITH OPEN COLLECTOR HIGH VOLTAGE OUTPUTS (max. 30 V; fan out = 25)

7407



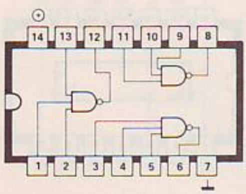
QUADRUPLE 2 INPUT AND GATES

7408
7409 open collector outputs



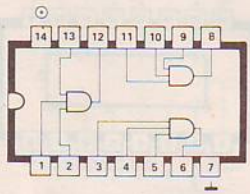
TRIPLE 3 INPUT NAND GATES

7410
7412 open collector outputs



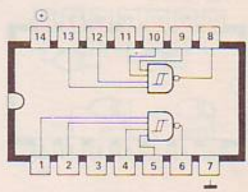
TRIPLE 3 INPUT AND GATE

7411



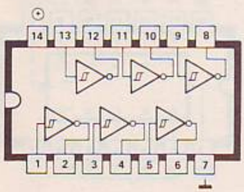
DUAL 4 INPUT NAND SCHMITT TRIGGER

7413



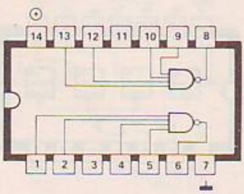
HEX SCHMITT TRIGGER INVERTER

7414



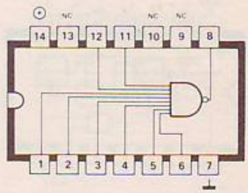
DUAL 4 INPUT NAND GATES

7420
7440 power driver (fan out = 30)



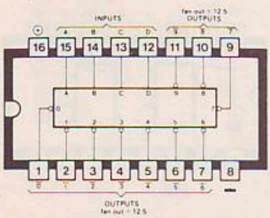
8 INPUT NAND GATE

7430



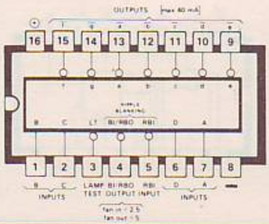
BCD TO DECIMAL DECODER/DRIVER WITH OPEN COLLECTOR OUTPUTS (max. 30 V)

7445



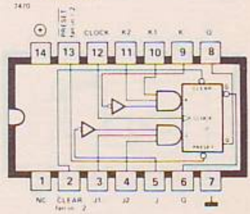
BCD TO 7 SEGMENT DECODER/DRIVER

7447



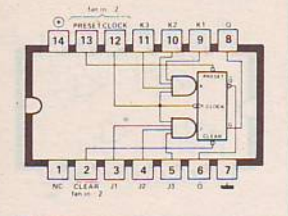
AND GATED J-K POSITIVE EDGE TRIGGERED FLIP FLOP WITH PRESET AND CLEAR

7470



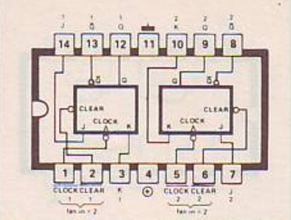
AND GATED J K FLIP FLOP WITH PRESET AND CLEAR

7472



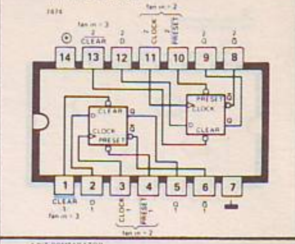
DUAL J K FLIP FLOP WITH CLEAR

7473



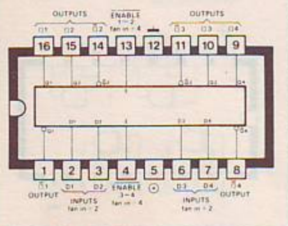
DUAL D TYPE POSITIVE EDGE TRIGGERED FLIP FLOP WITH PRESET AND CLEAR

7474



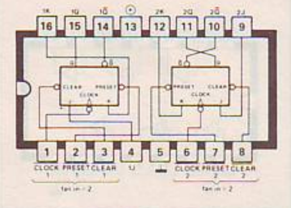
4 BIT BISTABLE LATCH

7475



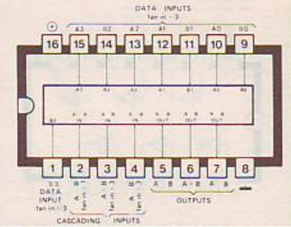
DUAL J K MASTER SLAVE FLIP FLOP WITH PRESET AND CLEAR

7476



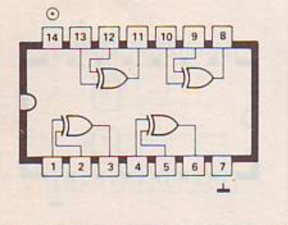
4 BIT COMPARATOR

7485



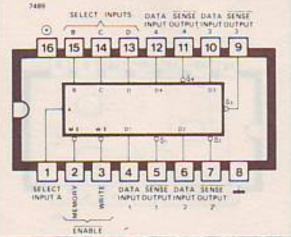
QUADRUPLE 2 INPUT EXCLUSIVE OR GATE

7486



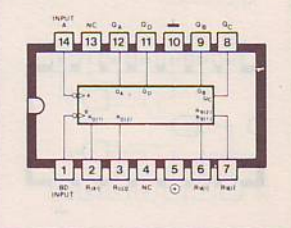
64 BIT READ WRITE MEMORY (fan out = 7.5)

7489



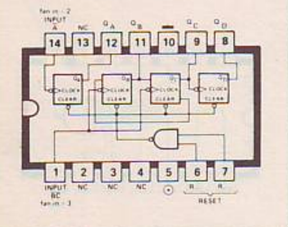
DECADE COUNTER

7490



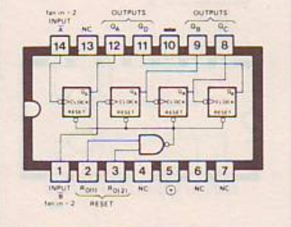
DIVIDE BY TWELVE COUNTER (÷ 2 and ÷ 6)

7492



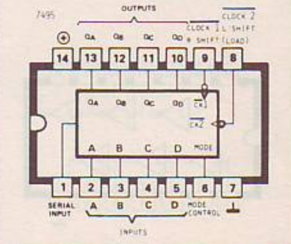
4 BIT BINARY COUNTER

7493



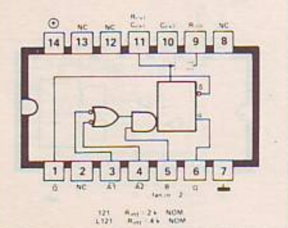
4-BIT PARALLEL-IN PARALLEL-OUT SHIFT REGISTER

7495



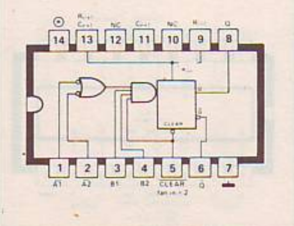
MONOSTABLE MULTIVIBRATOR

74121



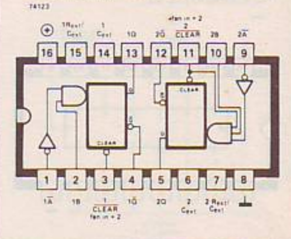
RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH CLEAR

74122



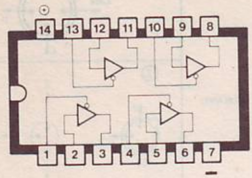
DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH CLEAR

74123



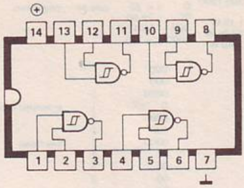
QUAD BUFFER (3 STATE)

74125



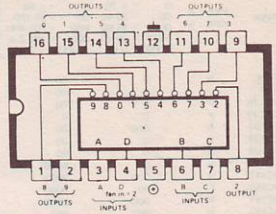
QUADRUPLE 2 INPUT NAND SCHMITT TRIGGER

74132



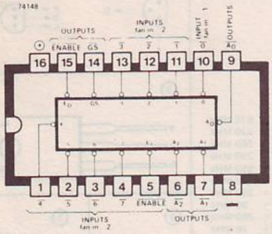
BCD TO DECIMAL DECODER DRIVER
(outputs max 60 V max 7 mA)

74141



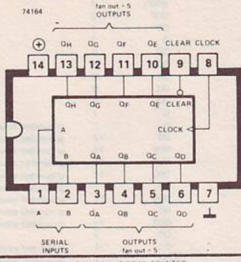
PRIORITY ENCODER

74148



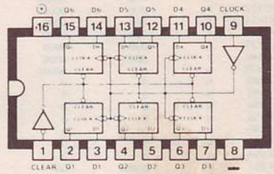
8 BIT SERIAL IN PARALLEL OUT SHIFT REGISTER

74164



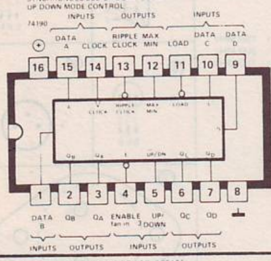
HEX D FLIP FLOP WITH CLEAR

74174



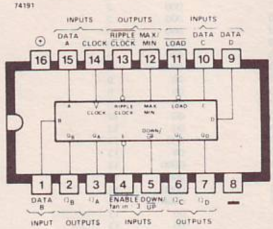
SYNCHRONOUS BCD UP DOWN COUNTER WITH UP DOWN MODE CONTROL

74190



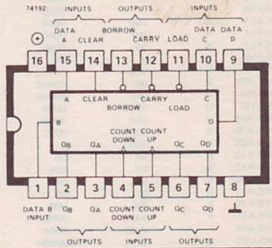
SYNCHRONOUS 4 BIT BINARY UP/DOWN COUNTER

74191



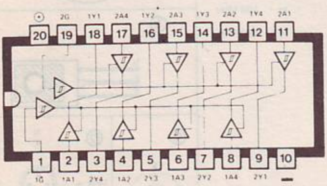
SYNCHRONOUS UP DOWN DECADE COUNTER

74192



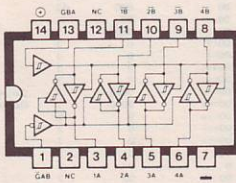
OCTAL BUFFER AND LINE DRIVER (3 STATE)

74LS241



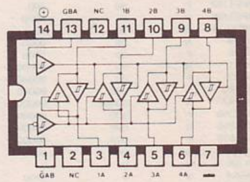
QUADRUPLE BUS TRANSCEIVER (3 STATE)

74LS242



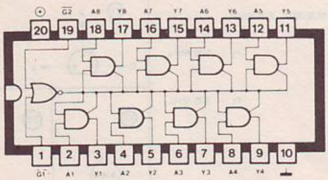
QUADRUPLE BUS TRANSCEIVER (3 STATE)

74LS243



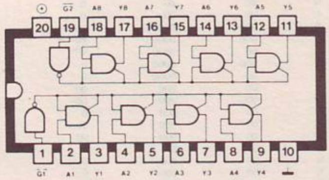
OCTAL BUFFER (3 STATE)

81LS95

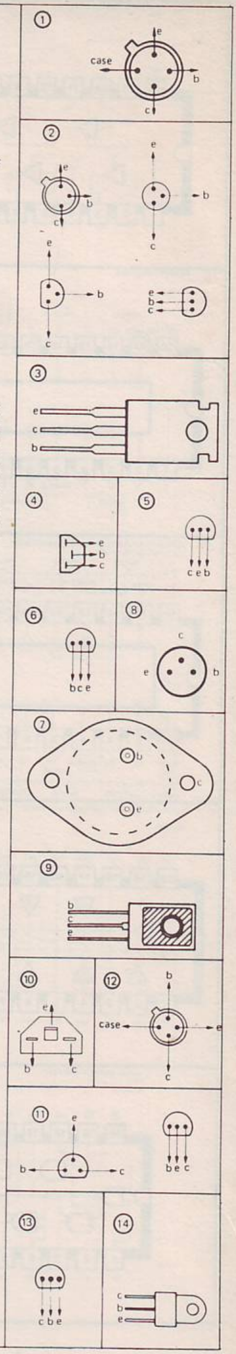


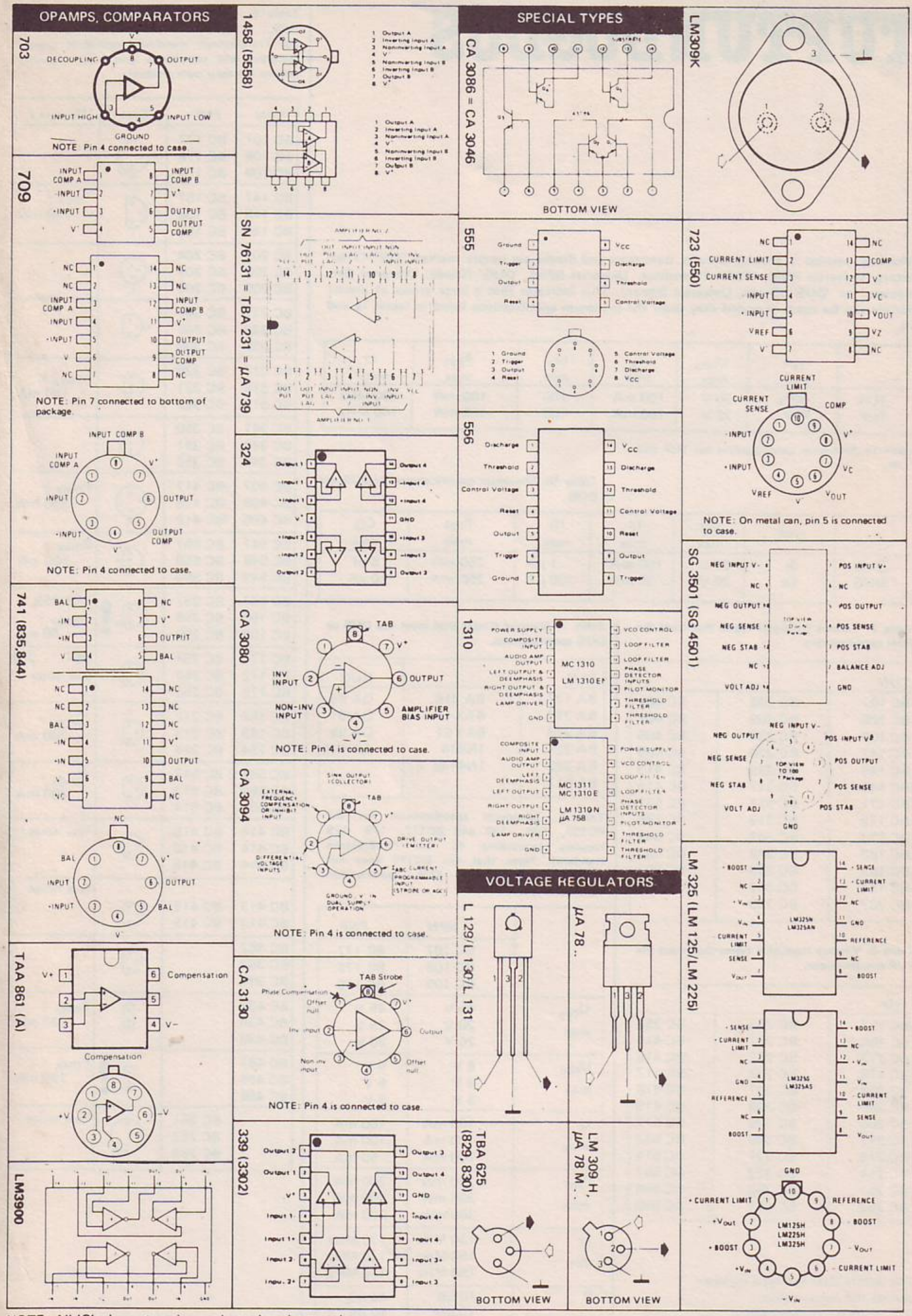
OCTAL BUFFER (3 STATE)

81LS97



Type	PNP = P NPN = N	U_{CEO} (Volt) 0 = ≤ 20 00 = 25-40 000 = 45-60 0000 = 65-80 00000 = ≥ 85	$I_{c(max)}$ (mA) 0 = ≤ 50 00 = 55-100 000 = 105-400 0000 = 405-2 A 00000 = ≥ 2 A	P_{max} (mW) not cooled: 0 = ≤ 300 00 = 305-1000 cooled: 00☆ = 1-10 W 00☆☆ = 10-35 W 00☆☆☆ = ≥ 40 W	$h_{FE(min)}$ 0 = ≤ 20 00 = 25-50 000 = 55-120 0000 = ≥ 125	case nr.	comments
TUN	N	0	00	0	000		
TUP	P	0	00	0	000		
AC126	P	0	00	00	0000	2	
AF239	P	0	0	0	0	1	grounded base: f f_T = 700 MHz
BC107	N	000	00	0	000	2	
BC108	N	0	00	0	000	2	
BC109	N	0	00	0	0000	2	low noise
BC140	N	00	0000	00☆	00	2	
BC141	N	000	0000	00☆	00	2	
BC160	P	00	0000	00☆	00	2	
BC161	P	000	0000	00☆	00	2	
BC182	N	000	000	0	0000	2	
BC212	P	000	000	0	000	2	
BC546	N	0000	00	00	0000	2	
BC556	P	0000	00	00	000	2	
BD106	N	00	00000	00☆☆	00	7	
BD130	N	000	00000	00☆☆☆	0	7	
BD132	P	000	00000	00☆☆	00	9	
BD137	N	000	0000	00☆	00	9	
BD138	P	000	0000	00☆	00	9	
BD139	N	0000	0000	00☆	00	9	
BD140	P	0000	0000	00☆	00	9	
BDY20	N	000	00000	00☆☆☆	0	7	
BF180	N	0	0	0	0	1	grounded base: f_T = 675 MHz
BF185	N	0	0	0	00	12	grounded base: f_T = 220 MHz
BF194	N	0	0	0	000	10	grounded emitter: f_T = 260 MHz
BF195	N	0	0	0	000	10	grounded emitter: f_T = 200 MHz
BF199	N	00	0	00	000	11	grounded emitter: f_T = 550 MHz
BF200	N	0	0	0	00	1	grounded base: f_T = 240 MHz
BF254	N	00	0	0	000	11	grounded emitter: f_T = 260 MHz
BF257	P	00000	00	00	00	2	grounded emitter: f_T = 90 MHz
BF494	N	0	0	0	000	11	grounded emitter: f_T = 260 MHz
BFX34	N	000	00000	00	00	2	f_T = 70 MHz
BFX89	N	0	0	0	00	1	grounded emitter: f_T = 1000 MHz
BFY90	N	0	0	0	00	1	grounded emitter: f_T = 1000 MHz
BSX19	N	0	0000	0	000	2	
BSX20	N	0	0000	0	000	2	
BSX61	N	000	0000	00	000	2	
HEP51	P	00	0000	00	000	1	f_T = 150 MHz
HEP53	N	00	0000	00	000	1	f_T = 200 MHz
HEP56	N	0	00	00	000	5	f_T = 750 MHz
MJE171	P	000	00000	00☆☆	00	9	
MJE180	N	00	00000	00☆☆	00	9	
MJE181	N	000	00000	00☆☆	00	9	
MJE340	N	00000	0000	00☆☆	00	9	
MPS A05	N	000	0000	00	00	13	
MPS A06	N	0000	0000	00	00	13	
MPS A09	N	0000	0	00	000	13	
MPS A10	N	00	00	00	00	13	
MPS A13	N	00	000	00	0000	13	
MPS A16	N	00	00	00	0000	13	
MPS A17	N	00	00	00	0000	13	
MPS A18	N	000	000	00	0000	13	
MPS A55	P	000	0000	0	00	13	
MPS A56	P	0000	0000	0	00	13	
MPS U01	N	00	00000	00☆	00	14	
MPS U05	N	000	00000	00☆	00	14	
MPS U56	P	0000	00000	00☆	00	14	
MPS2926	N	0	00	00	00	13	f_T = 300 MHz
MPS3394	N	00	00	00	000	13	
MPS3702	P	00	000	00	000	13	f_T = 100 MHz
MPS3706	N	0	0000	00	00	13	
MPS6514	N	00	00	0	0000	13	f_T = 480 MHz
TIP29	N	00	0000	00☆☆	0	3	
TIP30	P	00	0000	00☆☆	0	3	
TIP31	N	00	00000	00☆☆☆	0	3	
TIP32	P	00	00000	00☆☆☆	0	3	
TIP140	N	000	00000	00☆☆☆	0000	7	Darlington
TIP142	N	00000	00000	00☆☆☆	0000	7	Darlington
TIP2955	P	000	00000	00☆☆☆	0	3	
TIP3055	N	000	00000	00☆☆☆	0	3	
TIP5530	P	000	00000	00☆☆☆	0	3	
2N696	N	000	0000	00	0	2	
2N706	N	0	0	0	0	2	
2N914	N	0	0000	00	00	2	
2N1613	N	000	0000	00	00	2	
2N1711	N	000	0000	00	000	2	
2N1983	N	00	0000	00	000	2	
2N1984	N	00	0000	00		2	
2N2219	N	00	0000	00	00	2	
2N2222	N	00	0000	00	00	2	
2N2925	N	00	00	0	0000	13	
2N2955	P	00	00	0	0	2	≠ MJE2955, TIP2955!
2N3054	N	000	00000	00☆☆☆	00	7	
2N3055	N	000	00000	00☆☆☆	0	7	
2N3553	N	00	0000	00☆	0	2	f_T = 500 MHz
2N3568	N	000	0000	0	000	13	
2N3638	P	00	0000	0	000	13	
2N3702	P	00	000	00	000	13	
2N3866	N	00	000	00☆	0	2	f_T = 700 MHz
2N3904	N	00	000	0	00	13	
2N3905	P	00	000	00	000	13	
2N3906	P	00	000	00	000	13	
2N3907	N	000	0	0	000	13	
2N4123	N	00	000	0	00	13	
2N4124	N	00	000	0	000	13	
2N4126	P	00	000	0	000	13	
2N4401	N	00	0000	00	0	13	
2N4410	N	0000	000	00	000	13	
2N4427	N	0	000	00☆	0	2	f_T = 700 MHz
2N5183	N	0	0000	00	000	2	





NOTE: All IC's shown top view, unless otherwise stated.

TUPTUNDUGDUS

Wherever possible in Elektor circuits, transistors and diodes are simply marked 'TUP' (Transistors, Universal PNP), 'TUN' (Transistor, Universel NPN), 'DUG' (Diode, Universal Germanium) or 'DUS' (Diode, Universal Silicon). This indicates that a large group of similar devices can be used, provided they meet the minimum specifications listed in tables 1a and 1b.

	type	U_{ceo} max	I_c max	h_{fe} min.	P_{tot} max	f_T min.
TUN	NPN	20 V	100 mA	100	100 mW	100 MHz
TUP	PNP	20 V	100 mA	100	100 mW	100 MHz

Table 1a. Minimum specifications for TUP and TUN.

Table 1b. Minimum specifications for DUS and DUG.

	type	U_R max	I_F max	I_R max	P_{tot} max	C_D max
DUS	Si	25 V	100 mA	1 µA	250 mW	5 pF
DUG	Ge	20 V	35 mA	100 µA	250 mW	10 pF

Table 2. Various transistor types that meet the TUN specifications.

TUN		
BC 107	BC 208	BC 384
BC 108	BC 209	BC 407
BC 109	BC 237	BC 408
BC 147	BC 238	BC 409
BC 148	BC 239	BC 413
BC 149	BC 317	BC 414
BC 171	BC 318	BC 547
BC 172	BC 319	BC 548
BC 173	BC 347	BC 549
BC 182	BC 348	BC 582
BC 183	BC 349	BC 583
BC 184	BC 382	BC 584
BC 207	BC 383	

Table 3. Various transistor types that meet the TUP specifications.

TUP		
BC 157	BC 253	BC 352
BC 158	BC 261	BC 415
BC 177	BC 262	BC 416
BC 178	BC 263	BC 417
BC 204	BC 307	BC 418
BC 205	BC 308	BC 419
BC 206	BC 309	BC 512
BC 212	BC 320	BC 513
BC 213	BC 321	BC 514
BC 214	BC 322	BC 557
BC 251	BC 350	BC 558
BC 252	BC 351	BC 559

The letters after the type number denote the current gain:

A: α' (β, h_{fe}) = 125-260
B: α' = 240-500
C: α' = 450-900.

Table 4. Various diodes that meet the DUS or DUG specifications.

DUS		DUG
BA 127	BA 318	OA 85
BA 217	BAX 13	OA 91
BA 218	BAY 61	OA 95
BA 221	1N914	AA 116
BA 222	1N4148	
BA 317		

Table 5. Minimum specifications for the BC107, -108, -109 and BC177, -178, -179 families (according to the Pro-Electron standard). Note that the BC179 does not necessarily meet the TUP specification ($I_{c,max}$ = 50 mA).

	NPN	PNP
	BC 107 BC 108 BC 109	BC 177 BC 178 BC 179
U_{ceo} max	45 V 20 V 20 V	45 V 25 V 20 V
U_{ebo} max	6 V 5 V 5 V	5 V 5 V 5 V
I_c max	100 mA 100 mA 100 mA	100 mA 100 mA 50 mA
$P_{tot.}$ max	300 mW 300 mW 300 mW	300 mW 300 mW 300 mW
f_T min.	150 MHz 150 MHz 150 MHz	130 MHz 130 MHz 130 MHz
F max	10 dB 10 dB 4 dB	10 dB 10 dB 4 dB

Table 6. Various equivalents for the BC107, -108, . . . families. The data are those given by the Pro-Electron standard; individual manufacturers will sometimes give better specifications for their own products.

NPN	PNP	Case	Remarks
BC 107 BC 108 BC 109	BC 177 BC 178 BC 179		
BC 147 BC 148 BC 149	BC 157 BC 158 BC 159		P_{max} = 250 mW
BC 207 BC 208 BC 209	BC 204 BC 205 BC 206		
BC 237 BC 238 BC 239	BC 307 BC 308 BC 309		
BC 317 BC 318 BC 319	BC 320 BC 321 BC 322		I_{cmax} = 150 mA
BC 347 BC 348 BC 349	BC 350 BC 351 BC 352		
BC 407 BC 408 BC 409	BC 417 BC 418 BC 419		P_{max} = 250 mW
BC 547 BC 548 BC 549	BC 557 BC 558 BC 559		P_{max} = 500 mW
BC 167 BC 168 BC 169	BC 257 BC 258 BC 259	!	169/259 I_{cmax} = 50 mA
BC 171 BC 172 BC 173	BC 251 BC 252 BC 253		251 . . . 253 low noise
BC 182 BC 183 BC 184	BC 212 BC 213 BC 214		I_{cmax} = 200 mA
BC 582 BC 583 BC 584	BC 512 BC 513 BC 514		I_{cmax} = 200 mA
BC 414 BC 414 BC 414	BC 416 BC 416 BC 416		low noise
BC 413 BC 413	BC 415 BC 415		low noise
BC 382 BC 383 BC 384			
BC 437 BC 438 BC 439			P_{max} = 220 mW
BC 467 BC 468 BC 469		!	P_{max} = 220 mW
	BC 261 BC 262 BC 263		low noise